

Fast CMOS Bus Interface Latches

Product Features:

- PI74FCT841/843/845/2841T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

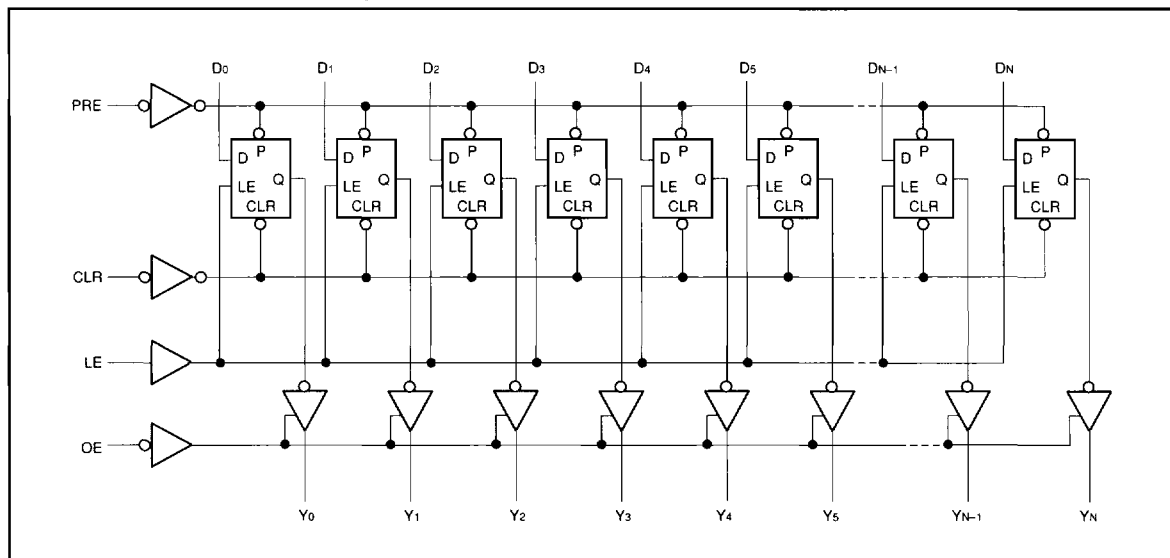
Product Description:

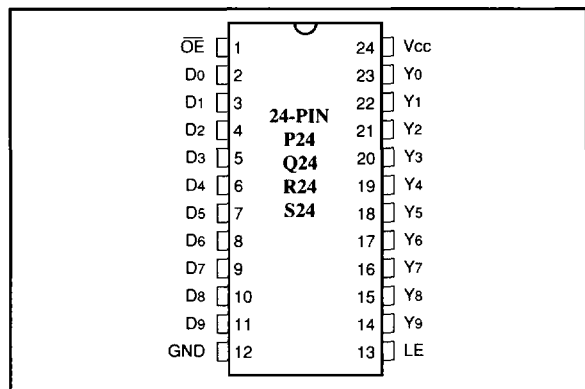
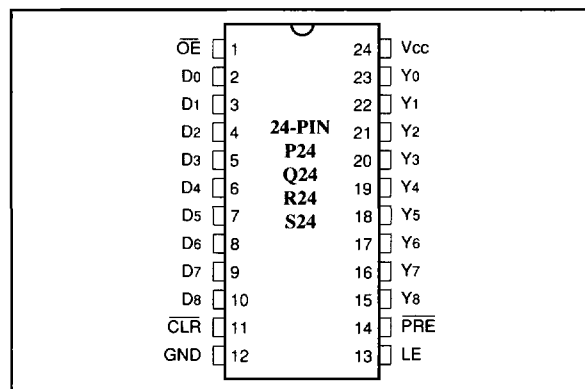
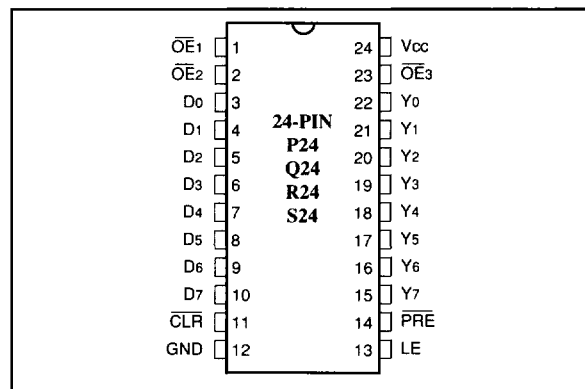
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25-ohm series resistor on all outputs to reduce noise because of reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT841T/843T/845T and PI74FCT2841T series are buffered interface latches. These transparent latches designed with 3-state outputs and are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The PI74FCT841/2841T is a 10-bit latch, the PI74FCT843T is a 9-bit latch, and the PI74FCT845T is an 8-bit latch.

PI74FCT841/843/845/2842T Logic Block Diagram



PI74FCT841/2841T 10-Bit Latch
Product Configuration

PI74FCT843T 9-Bit Latch Product Configuration

PI74FCT845T 8-Bit Latch Product Configuration

Product Pin Description

Pin Name	Description
YN	3-State Latch Outputs
DN	Latch Data Inputs
IE	Latch Enable Input
OE	Output Enable Control
CLR	Clear Latch
PRE	Preset Latch High, Preset Overrides CLR
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Function	Inputs					Outputs	Internal
	CLR	PRE	OE	IE	DN	YN	QN
High-Z	H	H	H	X	X	Z	X
	H	H	H	H	L	Z	L
	H	H	H	H	H	Z	H
Latched (High Z)	H	H	H	L	X	Z	NC
	H	H	L	H	L	L	L
Transparent	H	H	L	H	H	H	H
	H	H	L	L	X	NC	NC
Latched	H	H	L	L	X	NC	NC
Preset	H	L	L	X	X	H	H
Clear	L	H	L	X	X	L	L
Preset	L	L	L	X	X	H	H
Latched (High Z)	L	H	H	L	X	Z	L
Latched (High Z)	H	L	H	L	X	Z	H

1. H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 NC = No Change
 Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 48 mA		0.3	0.50	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 12 mA (25Ω Series)		0.3	0.50	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IiH	Input HIGH Current	VCC = Max.	VIN = VCC			1	μA
IiL	Input LOW Current	VCC = Max.	VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max.	VOUT = 2.7V			1	μA
IOZL	Output Current		VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA			-0.7	-1.2	V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120		mA
VH	Input Hysteresis				200		mV

Capacitance(TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN=0V	6	10	pF
COUT	Output Capacitance	VOUT=0V	8	12	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	500	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE = GND; LE = V _{cc} One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND; LE = V _{cc} fi = 5 MHz One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		1.5	3.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.8	4.5 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND; LE = V _{cc} Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		3.0	6.0 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		5.0	14.0 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{CP}/2 + f_i N_i)$$

I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT841/2841T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	841AT/2841AT		841BT/2841BT		841CT/2841CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay D _N to Y _N (LE = HIGH)	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
t _{SU}	Setup Time Data to LE	C _L = 50 pF R _L = 500Ω	2.5	—	2.5	—	2.5	—	ns
t _H	Hold Time Data to LE		2.5	—	2.5	—	2.5	—	ns
t _{PLH} t _{PHL}	Propagation Delay LE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	—	16.0	—	15.5	—	15.0	ns
t _W	LE Pulse Width ⁽³⁾ (HIGH)	C _L = 50 pF R _L = 500Ω	4.0	—	4.0	—	4.0	—	ns
t _{PZH} t _{PZL}	Output Enable Time OE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	ns
		C _L = 5 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT843T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	843AT		843BT		843CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay D _N to Y _N (LE = HIGH)	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
t _{SU}	Setup Time Data to LE	C _L = 50 pF R _L = 500Ω	2.5	—	2.5	—	2.5	—	ns
t _H	Hold Time Data to LE		2.5	—	2.5	—	2.5	—	ns
t _{PLH} t _{PHL}	Propagation Delay LE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	ns
t _{PLH}	Propagation Delay PRE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	11.0	1.5	8.0	1.5	7.0	ns
t _{REM}	Recovery Time PRE to Y _N		1.5	11.0	1.5	10.0	1.5	9.0	ns
t _{PLH}	Propagation Delay CLR to Y _N		1.5	11.0	1.5	10.0	1.5	9.0	ns
t _{REM}	Recovery Time ⁽³⁾ CLR to Y _N		1.5	13.0	1.5	10.0	1.5	9.0	ns
t _W	LE Pulse Width ⁽³⁾ (HIGH)		4.0	—	4.0	—	4.0	—	ns
t _W	PRE Pulse Width ⁽³⁾ (LOW)		5.0	—	4.0	—	4.0	—	ns
t _W	CLR Pulse Width ⁽³⁾ (LOW)		4.0	—	4.0	—	4.0	—	ns
t _{PZH} t _{PZL}	Output Enable Time OE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OE to Y _N	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	5.7	ns
		C _L = 5 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT845T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	845AT		845BT		845CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay DN to YN (LE = HIGH)	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
tsu	Setup Time Data to LE	CL = 50 pF RL = 500Ω	2.5	—	2.5	—	2.5	—	ns
th	Hold Time Data to LE		2.5	—	2.5	—	2.5	—	ns
tPLH tPHL	Propagation Delay LE to YN	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	ns
tPLH	Propagation Delay PRE to YN	CL = 50 pF RL = 500Ω	1.5	11.0	1.5	8.0	1.5	7.0	ns
tREM	Recovery Time ⁽³⁾ PRE to YN		1.5	11.0	1.5	10.0	1.5	9.0	ns
tPLH	Propagation Delay CLR to YN		1.5	11.0	1.5	10.0	1.5	9.0	ns
tREM	Recovery Time ⁽³⁾ CLR to YN		1.5	13.0	1.5	10.0	1.5	9.0	ns
tw	LE Pulse Width ⁽³⁾ (HIGH)		4.0	—	4.0	—	4.0	—	ns
tw	PRE Pulse Width ⁽³⁾ (LOW)		5.0	—	4.0	—	4.0	—	ns
tw	CLR Pulse Width ⁽³⁾ (LOW)		4.0	—	4.0	—	4.0	—	ns
tPZH tPZL	Output Enable Time OE to YN	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OE to YN	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	6.5	1.5	5.7	ns
		CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.