PI49FCT805T
PI49FCT2805T

Fast CMOS Clock Driver/Buffer

Features

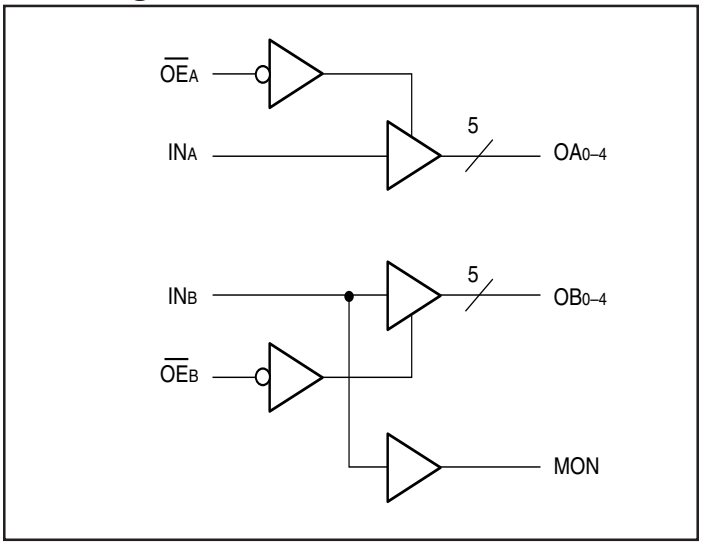
- Extremely low output skew: 0.5ns
- Monitor output pin
- Clock busing with Hi-Z state control
- TTL input and CMOS output compatible
- Extremely low static power (1mW, typ.)
- Hysteresis on all inputs
- Device models available on request
- Industrial Operation at -40ºC to +85ºC
- Packaging (Pb-free & Green available):
  – 20-pin 209-mil wide SSOP (H)
  – 20-pin 300-mil wide SOIC (S)
  – 20-pin 150-mil wide QSOP (Q)

Description

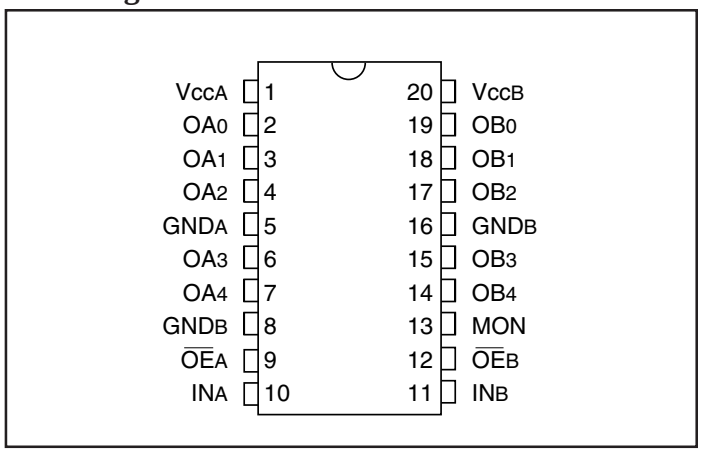
Pericom Semiconductor's PI49FCT805T and PI49FCT2805T are non-inverting clock drivers. Each clock driver consists of two banks of drivers, driving five outputs each from a standard TTL-compatible CMOS input.

The PI49FCT2805T features a 25-ohm on-chip resistor for lower noise.

Block Diagram



Pin Configuration



Truth Table[1]

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OA_N, OB_N	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

Note:
1. H= High Voltage Level
   L = Low Voltage Level
   Z = High Impedance

Pin Description

Pin Name	Description
$\overline{OE}_A$, $\overline{OE}_B$	Hi-Z State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_N, OB_N	Clock Outputs (PI49FCT805T/PI49FCT2805T)
MON	Monitor Output
GND	Ground
V_{CC}	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = –40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = –24.0mA$	2.4	3.3		V
V_{OL}	Output LOW Current	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 64mA$		0.3	0.55	V
			$I_{OL} = 12mA$ (25Ω)		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	$V_{IN} = V_{CC}$			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{OZH}	High Impedance	V_{CC} = Max.	$V_{OUT} = V_{CC}$			1	µA
I_{OZL}	Output Current		V_{OUT} = GND			–1	µA
I_I	Input HIGH Current	V_{CC} = Max., $V_{IN} = V_{CC}$ (Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., $I_{IN} = –18mA$			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120	–225	mA
V_H	Input Hysteresis	$V_{CC} = 5V$			200		mV

Capacitance ($T_A = 25°C$, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}=GND or V_{CC}		3	30	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC}=Max.	V_{IN}=3.4V[3]		0.5	2.0	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC}=Max., Outputs Open $\overline{OE}_A$=$\overline{OE}_B$=GND Per Output Toggling 50% Duty Cycle	V_{IN}=V_{CC} V_{IN}=GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC}=Max., Outputs Open f_i=10 MHz 50% Duty Cycle $\overline{OE}_A$=$\overline{OE}_B$=GND Five Outputs Toggling	V_{IN}=V_{CC} V_{IN}=GND		7.7	14.0[5]	mA
			V_{IN}=3.4V V_{IN}=GND		8.0	15.0[5]	
		V_{CC}=Max., Outputs Open f_i=2.5 MHz 50% Duty Cycle $\overline{OE}_A$=$\overline{OE}_B$=GND Eleven Outputs Toggling	V_{IN}=V_{CC} V_{IN}=GND		4.3	8.4[5]	
			V_{IN}=3.4V V_{IN}=GND		4.8	10.4[5]	

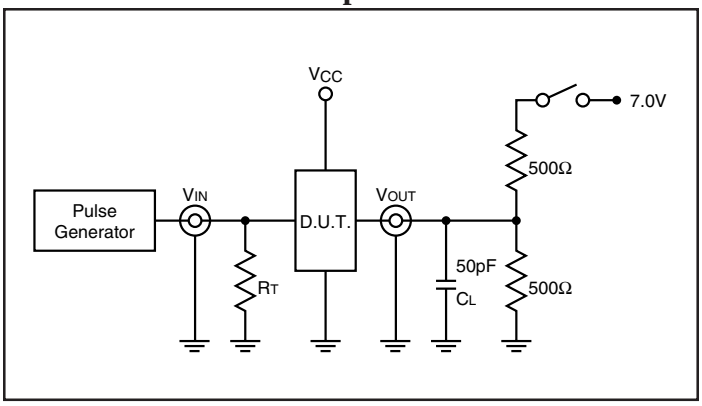
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_I = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	805T/2805T Com.		805AT/2805AT Com		805BT/2805BT Com.		805CT/2805CT Com		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_N, IN_B to OB_N	CL = 50pF RL = 500Ω	1.5	6.5	1.5	5.8	1.5	5.0	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_A$ to $\overline{OA}_N$, OE_B to OB_N		1.5	8.0	1.5	8.0	1.5	8.5	1.5	6.2	
t_{PHZ} t_{PLZ}	Output Disable Time[4] $\overline{OE}_A$ to $\overline{OA}_N$, OE_B to OB_N		1.5	7.0	1.5	7.0	1.5	6.0	1.5	5.0	
$t_{SKEW(o)}$[3]	Skew twx two outputs of same package (same transition)		—	0.7	—	0.5	—	0.4	—	0.4	
$t_{SKEW(p)}$[3]	Skew twx opposite transitions (t_{PHL}-t_{PLH}) of same output		—	1.0	—	0.7	—	0.5	—	0.5	
$t_{SKEW(t)}$[3]	Skew twx two outputs of different package at same temperature (same transition)		—	1.5	—	1.0	—	1.0	—	1.0	

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).
4. This parameter is guaranteed but not production tested.

Tests Circuits For All Outputs[1]



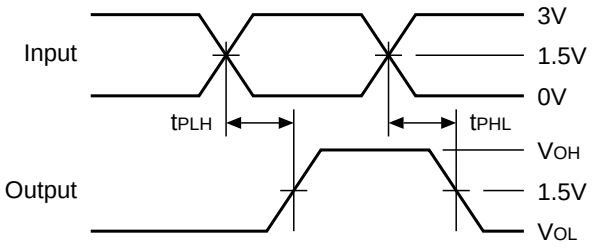
Switch Position

Test	Switch
Open Drain Disable LOW Enable LOW	Closed
All Other Inputs	Open

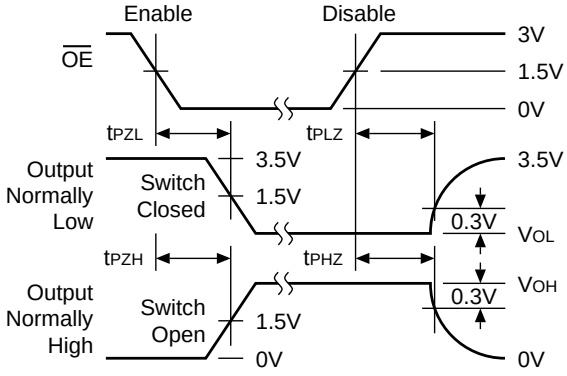
Definitions:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to ZOUT of the Pulse Generator.

Switching Waveforms

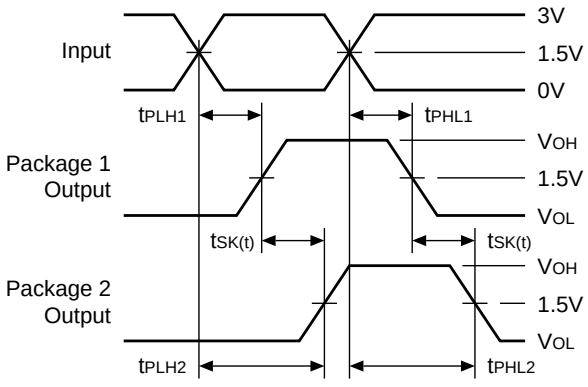
Propagation Delay



Enable and Disable Times

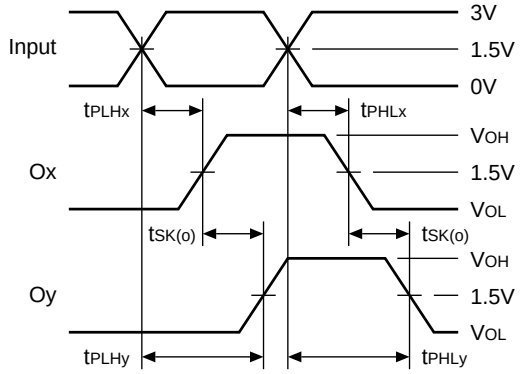


Package Skew – $t_{SK(t)}$



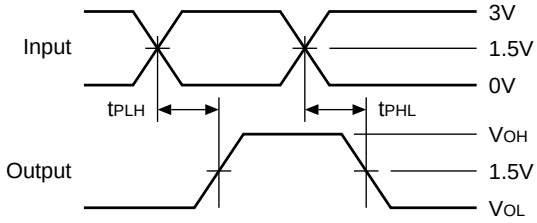
$t_{SK(t)} = | t_{PLH2} \quad t_{PLH1} |$ or $| t_{PHL2} \quad t_{PHL1} |$

Output Skew – $t_{SK(o)}$



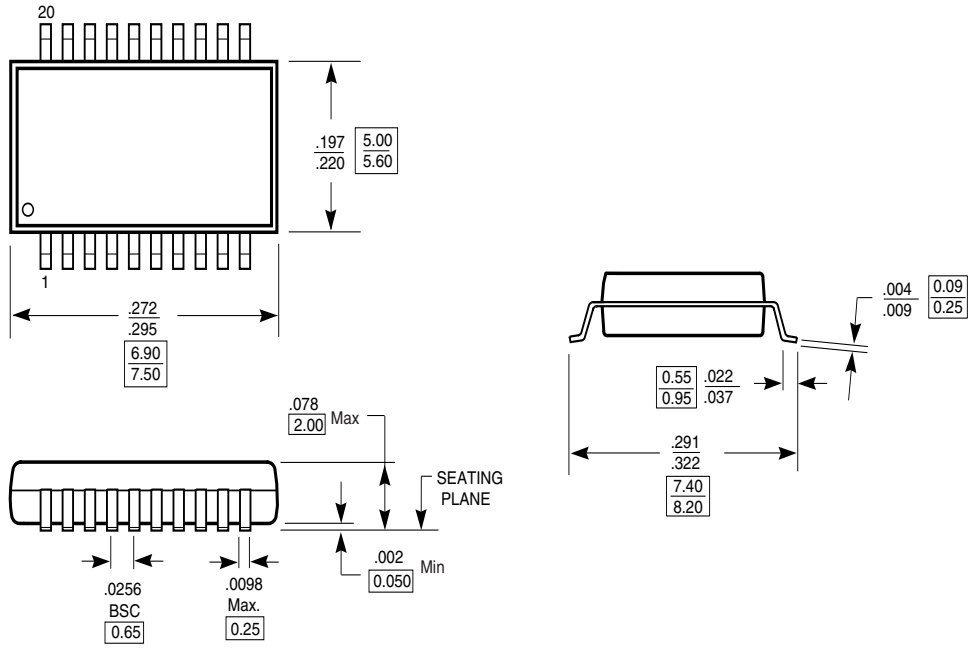
$t_{SK(o)} = | t_{PLHy} \quad t_{PLHx} |$ or $| t_{PHLy} \quad t_{PHLx} |$

Pulse Skew – $t_{SK(p)}$

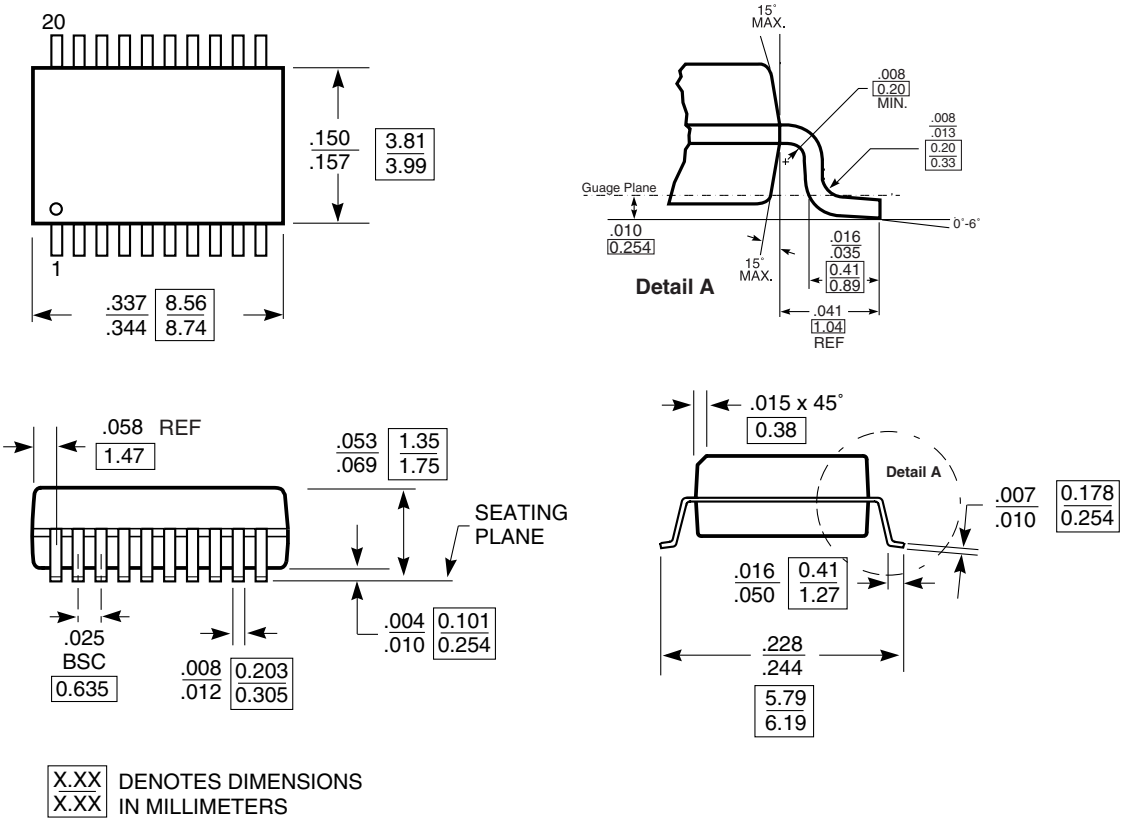


$t_{SK(p)} = | t_{PHL} \quad t_{PLH} |$

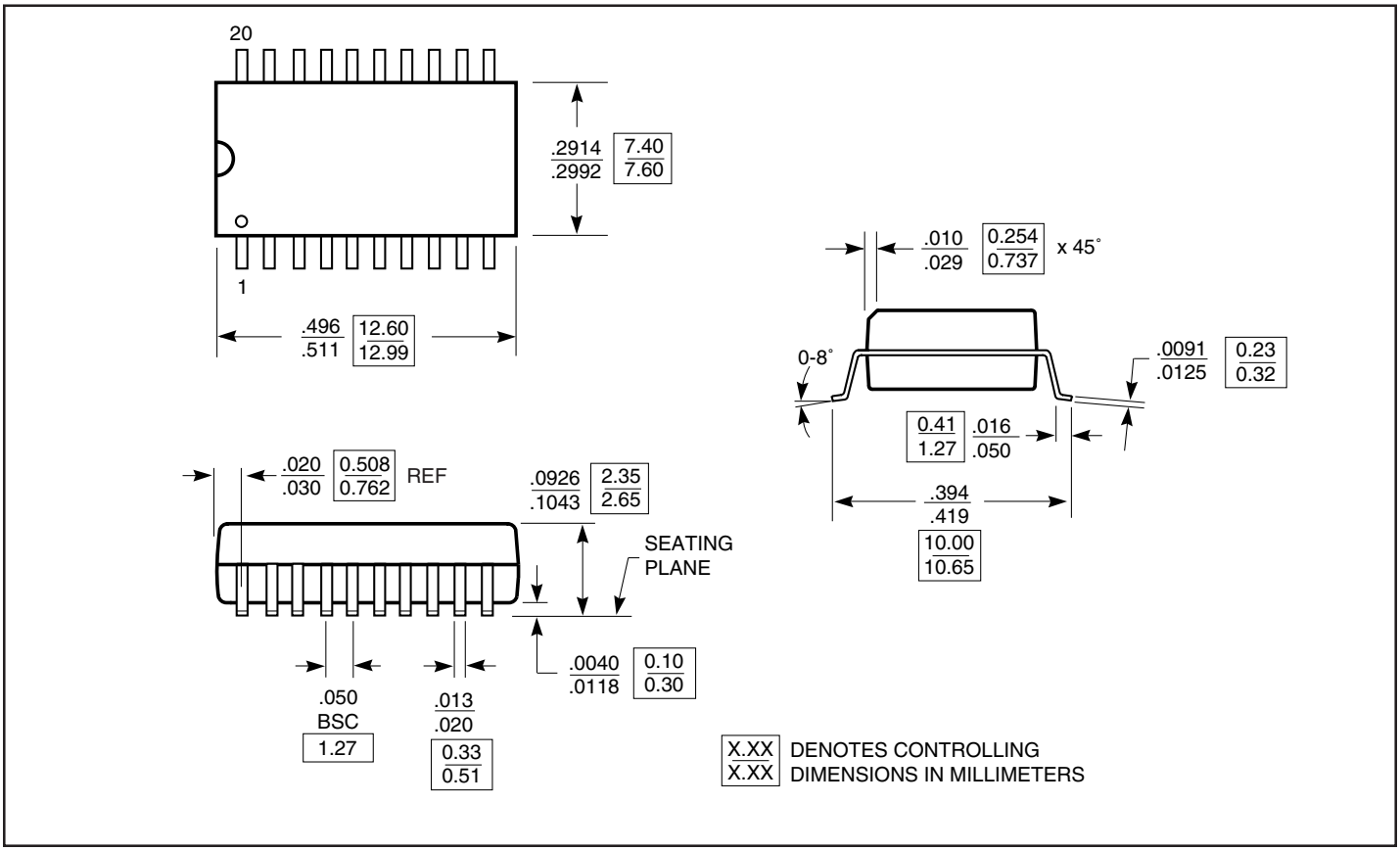
Packaging Mechanical: 20-Pin 209-Mil SSOP (H)



Packaging Mechanical: 20-Pin 150-Mil QSOP (Q)



Packaging Mechanical: 20-Pin 300-Mil SOIC (S)



Ordering Information for PI49FCT805T

Ordering Code	Package Code	Speed Grade	Package Type
PI49FCT805TS	S	Blank	20pin 300-mil SOIC
PI49FCT805TSE	S	Blank	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT805TH	H	Blank	20-pin 209-mil SOIC
PI49FCT805THE	H	Blank	Pb-free & Green, 20-pin 209-mil SOIC
PI49FCT805TQ	Q	Blank	20-pin 150-mil QSOP
PI49FCT805TQE	Q	Blank	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT805ATS	S	A	20pin 300-mil SOIC
PI49FCT805ATSE	S	A	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT805ATH	H	A	20-pin 209-mil SOIC
PI49FCT805ATHE	H	A	Pb-free & Green, 20-pin 209-mil SOIC
PI49FCT805ATQ	Q	A	20-pin 150-mil QSOP
PI49FCT805ATQE	Q	A	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT805BTS	S	B	20pin 300-mil SOIC
PI49FCT805BTSE	S	B	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT805BTH	H	B	20-pin 209-mil SOIC
PI49FCT805BTHE	H	B	Pb-free & Green, 20-pin 209-mil SOIC
PI49FCT805BTQ	Q	B	20-pin 150-mil QSOP
PI49FCT805BTQE	Q	B	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT805CTS	S	C	20pin 300-mil SOIC
PI49FCT805CTSE	S	C	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT805CTH	H	C	20-pin 209-mil SOIC
PI49FCT805CTHE	H	C	Pb-free & Green, 20-pin 209-mil SOIC
PI49FCT805CTQ	Q	C	20-pin 150-mil QSOP
PI49FCT805CTQE	Q	C	Pb-free & Green, 20-pin 150-mil QSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

Ordering Information for PI49FCT2805T

Ordering Code	Package Code	Speed Grade	Package Type
PI49FCT2805TS	S	Blank	20pin 300-mil SOIC
PI49FCT2805TSE	S	Blank	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT2805TQ	Q	Blank	20-pin 150-mil QSOP
PI49FCT2805TQE	Q	Blank	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT2805ATQ	Q	A	20-pin 150-mil QSOP
PI49FCT2805ATQE	Q	A	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT2805BTS	S	B	20pin 300-mil SOIC
PI49FCT2805BTSE	S	B	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT2805BTQ	Q	B	20-pin 150-mil QSOP
PI49FCT2805BTQE	Q	B	Pb-free & Green, 20-pin 150-mil QSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/