LP5951 Micropower, 150-mA Low-Dropout CMOS Voltage Regulator

1 Features

- Input Voltage Range: 1.8 V to 5.5 V
- Output Voltage Range: 1.3 V to 3.7 V
- Excellent Line Transient Response: ±2 mV (typical)
- Excellent PSRR: –60 dB at 1 kHz typical
- Low Quiescent Current of 29 µA typical
- Small SC70-5 and SOT-23-5 Packages
- Fast Turnon Time of 30 µs typ.
- Typical < 1 nA Quiescent Current in Shutdown
- Ensured 150-mA Output Current
- Logic Controlled Enable 0.4 V/0.9 V
- Good Load Transient Response of 50 mVpp (typical)
- Thermal Overload and Short-Circuit Protection
- -40°C to 125°C Junction Temperature Range

2 Applications

General Purpose

3 Description

The LP5951 regulator is designed to meet the requirements of portable battery-powered systems providing a regulated output voltage and low quiescent current. When switched to shutdown mode via a logic signal at the Enable (EN) pin, the power consumption is reduced to virtually zero.

The LP5951 is designed to be stable with small 1-µF ceramic capacitors. The device also features internal protection against short-circuit currents and over-temperature conditions.

Performance is specified for a –40°C to 125°C temperature range.

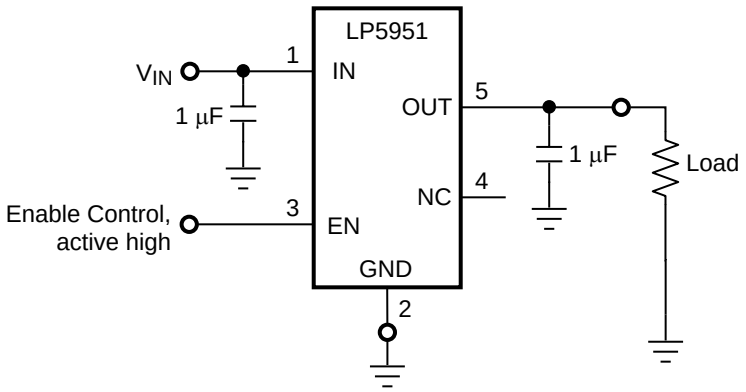
The device is available in fixed output voltages in the range of 1.3 V to 3.7 V. For availability, please contact your local TI sales office.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP5951	SOT-23 (5)	2.90 mm x 1.60 mm
	SC70 (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (May 2013) to Revision G — **Page**

- Added *Device Information* and *ESD Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; updated pin names; added new thermal information; moved some curves to *Application Curves* section ... 1
- Changed wording of footnote 2 ... 5
- Changed values of RθJA and "454 mW" to "511 mW" for SOT-23-5 package ... 10

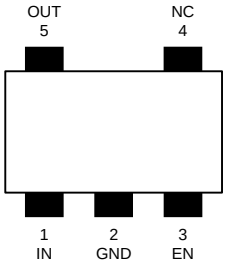
Changes from Revision E (April 2013) to Revision F — **Page**

- Changed layout of National Data Sheet to TI format ... 12

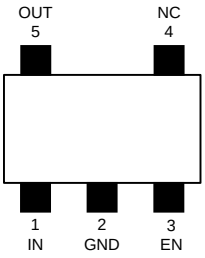
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5 Pin Configuration and Functions

SOT-23 (DBV)
5 Pins
Top View



SC70 (DCK)
5 Pins
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	IN	I	Input voltage 1.8 V to 5.5 V
2	GND	—	Ground
3	EN	I	Enable pin logic input: Low = shutdown, High = normal operation. This pin should not be left floating.
4	NC	—	No internal connection
5	OUT	O	Regulated output voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

	MIN	MAX	UNIT
IN pin: Voltage to GND	–0.3	6.5	V
EN pin: Voltage to GND	–0.3 to (V_{IN} + 0.3 V)(2)	6.5	
Continuous power dissipation(3)	Internally limited		
Junction temperature (T_{J-MAX})		150	°C
Package peak reflow temperature (10-20 s)		240	
Package peak reflow temperature (Pb-free, 10-20 s)		260	
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The lower of V_{IN} + 0.3 or 6.5 V.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 140°C (typ.).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.8		5.5	V
V_{EN}	Enable input voltage	0		(V_{IN} + 0.3)	V
T_J	Junction temperature	–40		125	°C
T_A	Ambient temperature	See Power Dissipation And Device Operation			

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.

6.4 Thermal Information

THERMAL METRIC(1)		LP5951		UNIT
		SOT-23 (DBV)	SC70 (DCK)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	195.6	276.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	108.3	86.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	52.1	56.9	
ψ_{JT}	Junction-to-top characterization parameter	11.0	1.3	
ψ_{JB}	Junction-to-board characterization parameter	51.6	56.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

All typical (TYP) values and limits are for $T_A = T_J = 25°C$, and minimum (MIN) and maximum (MAX) limits apply over the operating junction temperature range (T_J) of –40°C to 125°C unless otherwise specified in the Test Conditions. Unless otherwise noted, $V_{IN} = V_{OUT(NOM)} + 1$ V, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, $V_{EN} = 0.9$ V. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	$V_{IN} \geq V_{OUT(NOM)} + V_{DO}$	1.8		5.5	V
ΔV_{OUT}	Output voltage tolerance	I_{OUT} = 1mA T_J = 25°C	–2%		2%	
		I_{OUT} = 1mA –30°C ≤ T_J ≤ +125°C	–3.5%		3.5%	
	Line regulation error	$V_{IN} = V_{OUT(NOM)} + 1$ V to 5.5 V I_{OUT} = 1 mA		0.1		%/V
	Load regulation error	I_{OUT} = 1 mA to 150 mA		–0.01		%/mA
V_{DO}	Output voltage dropout(3)	I_{OUT} = 150 mA , $V_{OUT} \geq 2.5$ V			250	mV
		I_{OUT} = 150 mA , $V_{OUT} < 2.5$ V		200	350	
I_Q	Quiescent current	V_{EN} = 0.9 V, I_{LOAD} = 0		29	55	µA
		V_{EN} = 0.9 V, I_{LOAD} = 150 mA		33	70	
		V_{EN} = 0 V, T_J = 25°C		0.005	1	
I_{SC}	Output current (short circuit)	$V_{IN} = V_{OUT(NOM)} + 1$ V	150	400		mA
PSRR	Power supply rejection ratio	Sine modulated V_{IN}, f = 100 Hz		60		dB
		Sine modulated V_{IN}, f = 1 kHz		60		
		Sine modulated V_{IN}, f = 10 kHz		50		
E_N	Output noise	BW = 10 Hz - 100 kHz		125		μV_{RMS}
TSD	Thermal shutdown			160		°C
	Temperature hysteresis			20		

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and Maximum limits are ensured through test, design, or statistical correlation over the operating junction temperature range (T_J) of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.
(3) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100 mV below the nominal output voltage. This specification does not apply for output voltages below 1.8 V.

6.6 Enable Control Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EN}	Maximum input current at EN input	0 V ≤ V_{EN} ≤ V_{IN}, V_{IN} = 5.5 V –40°C ≤ T_J ≤ 125°C	–1		1	µA
V_{IL}	Low input threshold (shutdown)	V_{IN} = 1.8 V to 5.5 V –40°C ≤ T_J ≤ 125°C			0.4	V
V_{IH}	High input threshold (enable)	V_{IN} = 1.8 V to 5.5 V –40°C ≤ T_J ≤ 125°C	0.9			

6.7 Transient Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Dynamic line transient	$V_{IN} = V_{OUT(NOM)} + 1$ V to $V_{OUT(NOM)} + 1$ V + 0.6 V in 30 µs, no load		±2		mV
ΔV_{OUT}	Dynamic load transient	I_{OUT} = 0 mA to 150 mA in 10 µs I_{OUT} = 150 mA to 0 mA in 10 µs I_{OUT} = 1 mA to 150 mA in 1 µs I_{OUT} = 150 mA to 1 mA in 1 µs		-30 20 -50 40		mV mV mV mV
ΔV_{OUT}	Overshoot on start-up	Nominal conditions		10		mV
T_{ON}	Turnon time	I_{OUT} = 1 mA		30		µs

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6.8 Output Capacitor, Recommended Specification

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
C_{OUT}	Output capacitance	Capacitance(2) I_{OUT} = 150 mA, V_{IN} = 5 V	0.7	1	47	µF
		ESR	0.003		0.300	Ω

(1) Min and Max limits are ensured by design.
(2) The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. The shown minimum limit represents real minimum capacitance, including all tolerances and must be maintained over temperature and dc bias voltage (see *External Capacitors* in *Application and Implementation* section).

6.9 Typical Characteristics

Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{OUT} = 1 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C; EN pin is tied to V_{IN}.

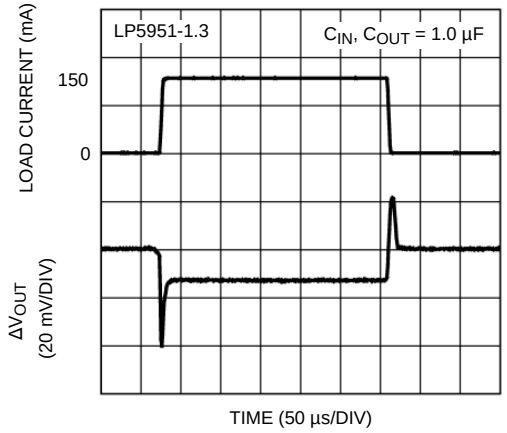


Figure 1. Load Transient Response

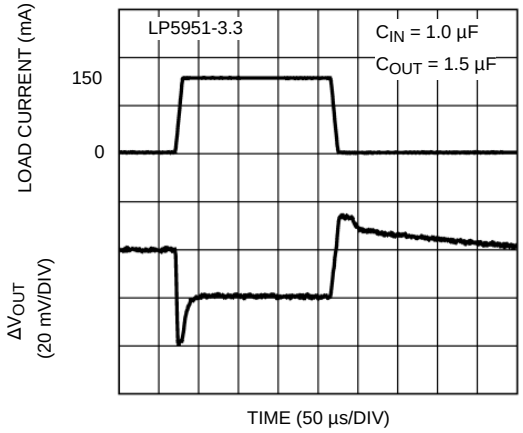


Figure 2. Load Transient Response

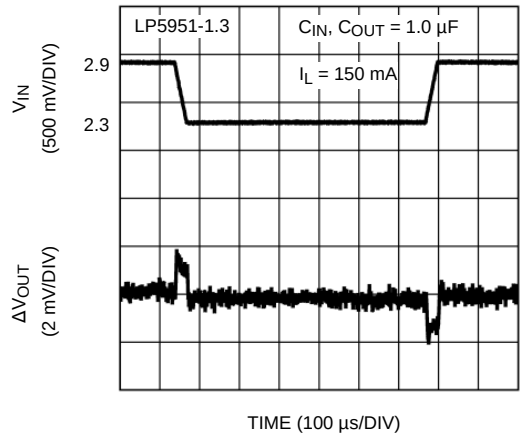


Figure 3. Line Transient Response

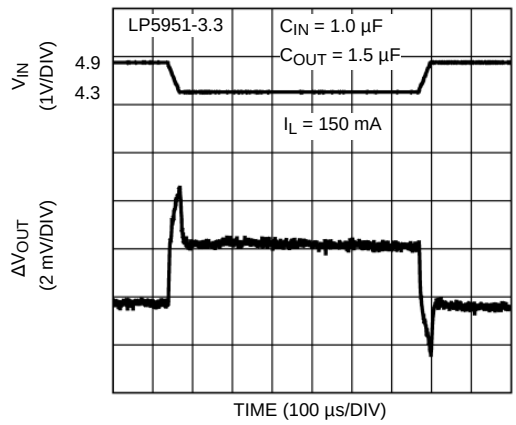


Figure 4. Line Transient Response

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Typical Characteristics (continued)

Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{OUT} = 1 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C; EN pin is tied to V_{IN}.

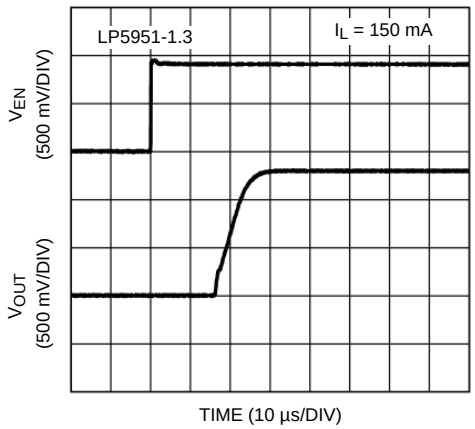


Figure 5. Enable Start-Up Time

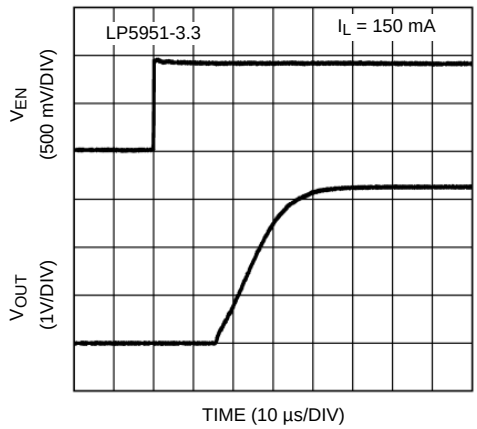


Figure 6. Enable Start-Up Time

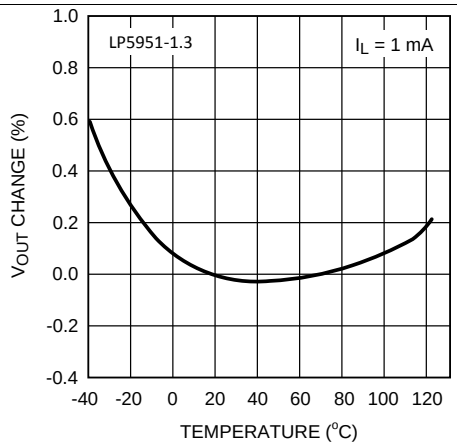


Figure 7. Output Voltage Change vs Temperature

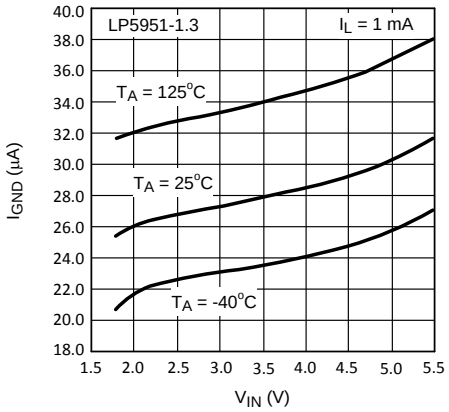


Figure 8. Ground Current vs V_{IN}

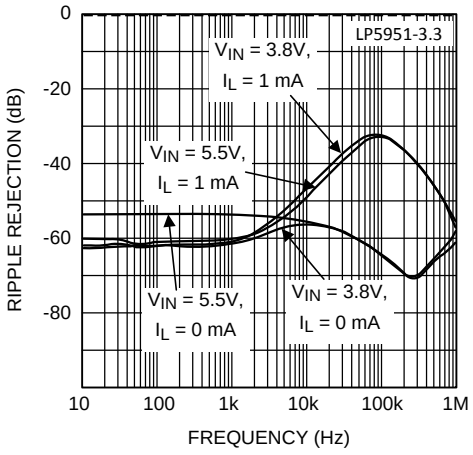


Figure 9. Power Supply Rejection Ratio

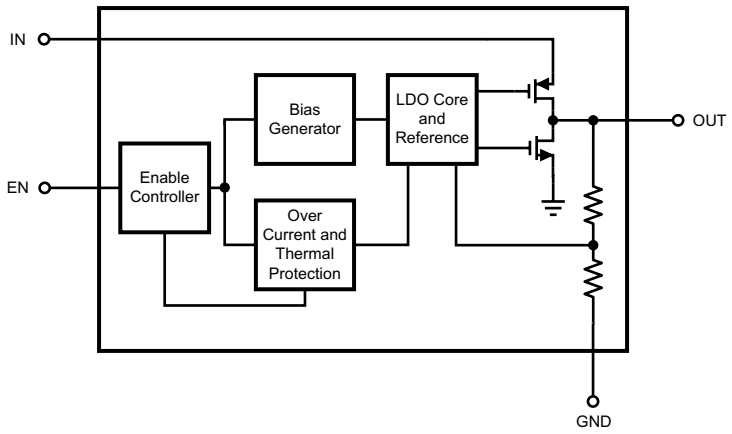
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7 Detailed Description

7.1 Overview

The LP5951 regulator is designed to meet the requirements of portable battery-powered systems providing a regulated output voltage and low quiescent current. When switched to shutdown mode via a logic signal at the EN pin, the power consumption is reduced to virtually zero.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 No-Load Stability

The LP5951 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

7.3.2 Enable Operation

The LP5951 may be switched ON or OFF by a logic input at the Enable pin, EN. A logic high at this pin will turn the device on. When the EN pin is low, the regulator output is off and the device typically consumes 5 nA.

If the application does not require the enable switching feature, the EN pin should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Enable Control Characteristics* table, V_{IL} and V_{IH}.

7.3.3 Fast Turn Off And On

The controlled switch-off feature of the device provides a fast turn off by discharging the output capacitor via an internal FET device. This discharge is current limited by the RDSon of this switch.

Fast turnon is ensured by an optimized architecture allowing a very fast ramp of the output voltage to reach the target voltage.

7.3.4 Short-Circuit Protection

The LP5951 is short circuit protected and in the event of a peak over-current condition, the output current through the PMOS will be limited.

If the over-current condition exists for a longer time, the average power dissipation will increase depending on the input to output voltage difference until the thermal shutdown circuitry will turn off the PMOS.

Please refer to the *Thermal Information* section for power dissipation calculations.

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Feature Description (continued)

7.3.5 Thermal-Overload Protection

Thermal-Overload Protection limits the total power dissipation in the LP5951. When the junction temperature exceeds T_J = 160°C typ., the shutdown logic is triggered and the PMOS is turned off, allowing the device to cool down. After the junction temperature dropped by 20°C (temperature hysteresis), the PMOS is activated again. This results in a pulsed output voltage during continuous thermal-overload conditions.

The Thermal-Overload Protection is designed to protect the LP5951 in the event of a fault condition. For normal, continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = 150°C (see *Absolute Maximum Ratings*).

7.3.6 Reverse Current Path

The internal PFET pass device in LP5951 has an inherent parasitic body diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 50 mA.

For currents above this limit an external Schottky diode must be connected from V_{OUT} to V_{IN} (cathode on V_{IN}, anode on V_{OUT}).

7.4 Device Functional Modes

7.4.1 Enable (EN)

The EN pin voltage must be higher than the VIH threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the VIL threshold to ensure that the device is fully disabled. However if the application does not require the shutdown feature, the VEN pin can be tied to VIN to keep the regulator output permanently on.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5951 internal circuitry is not fully functional until V_{IN} is at least 1.8 V. The output voltage is not regulated until $V_{IN} \geq (V_{OUT} + V_{DO})$, or 1.8 V, whichever is higher.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5951 is a linear voltage regulator for digital applications designed to be stable with space-saving ceramic capacitors as small as 1 µF. Performance is specified for a -40°C to 125°C temperature range for bot the SOT-23 and SC70 packages.

8.2 Typical Application

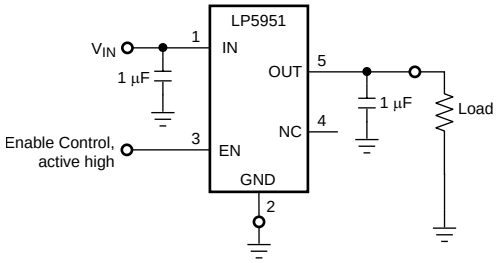


Figure 10. LP5951 Typical Application

8.2.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	DESIGN REQUIREMENT
Input voltage range	1.8 V to 5.5 V
Output voltage	1.3 V
Output current	150 mA
Output capacitor range	1 µF
Input/output capacitor ESR range	3 mΩ to 300 mΩ

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation And Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

The allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = (T_{J(MAX)} – T_A) / R_{\theta JA} \quad (1)$$

With an $R_{\theta JA}$ = 195.6°C/W, the device in the SOT-23-5 package returns a value of 511 mW with a maximum junction temperature of 125°C at T_A of 25°C.

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The actual power dissipation across the device can be estimated by the following equation:

$$P_D \approx (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

8.2.2.2 External Capacitors

As is common with most regulators, the LP5951 requires external capacitors to ensure stable operation. The LP5951 is specifically designed for portable applications requiring minimum board space and the smallest size components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LP5951 IN pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≥ 0.7 µF over the entire operating temperature range.

8.2.2.4 Output Capacitor

The LP5951 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X7R, Z5U, or Y5V) in the 1-µF range (up to 47 µF) and with ESR between 3 mΩ to 500 mΩ is suitable in the LP5951 application circuit.

This capacitor must be located a distance of not more than 1 cm from the OUT pin and returned to a clean analogue ground.

It is also possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

8.2.2.5 Capacitor Characteristics

The LP5951 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 3 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5951.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 11 shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7 µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (such as 0402) may not be suitable in the actual application.

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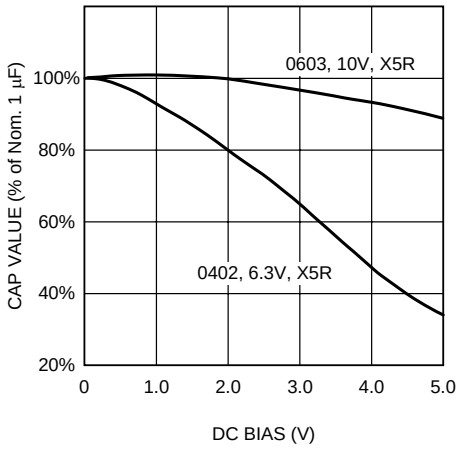


Figure 11. Typical Variation in Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of –55°C to 125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of –55°C to 85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

Table 2. Suggested Capacitors and Their Suppliers

CAPACITANCE / µF	MODEL	VENDOR	TYPE	CASE SIZE / INCH (mm)
1	C1608X5R1A105K	TDK	Ceramic, X5R	0603 (1608)
1	C1005X5R1A105K	TDK	Ceramic, X5R	0402 (1005)

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8.2.3 Application Curves

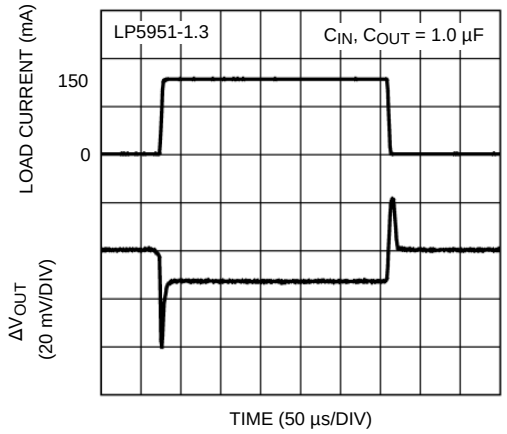


Figure 12. Load Transient Response

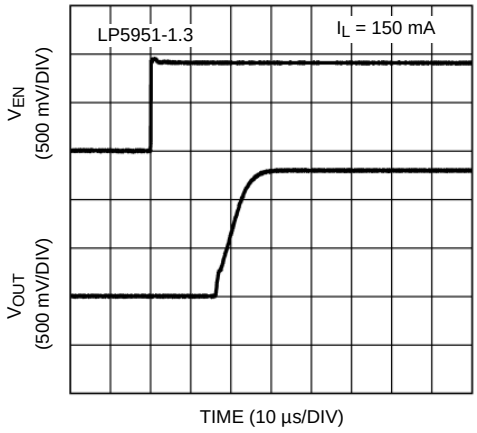


Figure 13. Enable Start-Up Time

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.8 V to 5.5 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP5951 output voltage is well regulated, the input supply should be at least V_{OUT} + 0.5 V, or 1.8 V, whichever is higher. A minimum capacitor value of 1-µF is required to be within 1 cm of the IN pin.

9.1 Output Current Derating

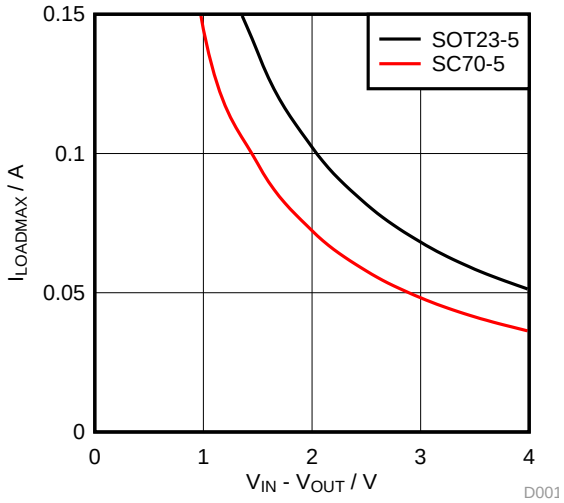


Figure 14. Maximum Load Current vs V_{IN} – V_{OUT}, T_A = 85°C, V_{OUT} = 1.5 V

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5951 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the load regulation, PSRR, noise, or transient performance of the LP5951. Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5951, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LP5951 ground pin using as wide, and as short, of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

A Ground Plane, either on the opposite side of a two-layer PCB, or embedded in a multi-layer PCB, is strongly recommended. This Ground Plane serves as a circuit reference plane to assure accuracy.

10.2 Layout Example

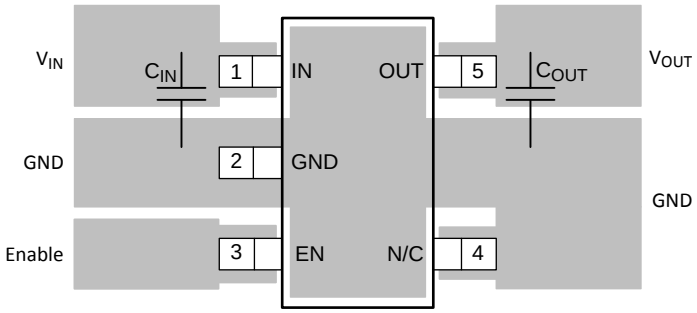


Figure 15. LP5951 Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For the availability of evaluation boards, see the LP5951 product folder. For information regarding evaluation boards, see the TI AN-1486 Application Report *LP5951 Evaluation Board* (SNVA169).

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5951MF-1.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKRB	Samples
LP5951MF-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKAB	Samples
LP5951MF-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKBB	Samples
LP5951MF-2.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKCB	Samples
LP5951MF-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKEB	Samples
LP5951MF-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKFB	Samples
LP5951MF-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKGB	Samples
LP5951MF-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LKHB	
LP5951MF-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKHB	Samples
LP5951MFX-1.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKRB	Samples
LP5951MFX-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKAB	Samples
LP5951MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKBB	Samples
LP5951MFX-2.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKCB	Samples
LP5951MFX-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKEB	Samples
LP5951MFX-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKGB	Samples
LP5951MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKHB	Samples
LP5951MG-1.3/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L23	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5951MG-1.5/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L2B	Samples
LP5951MG-1.8/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L3B	Samples
LP5951MG-2.0/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L4B	Samples
LP5951MG-2.5/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L5B	Samples
LP5951MG-2.8/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L6B	Samples
LP5951MG-3.0/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L7B	Samples
LP5951MG-3.3/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LAB	Samples
LP5951MGX-1.3/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L23	Samples
LP5951MGX-1.5/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L2B	Samples
LP5951MGX-1.8/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L3B	Samples
LP5951MGX-2.5/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L5B	Samples
LP5951MGX-2.8/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L6B	Samples
LP5951MGX-3.0/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L7B	Samples
LP5951MGX-3.3/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LAB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

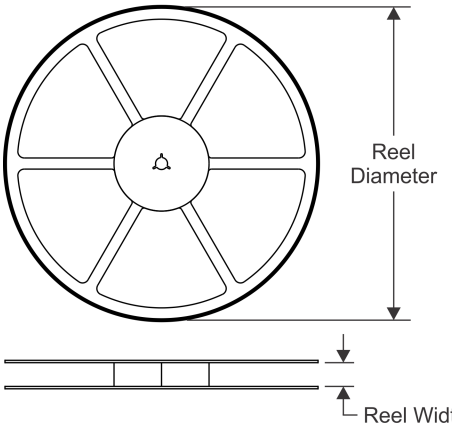
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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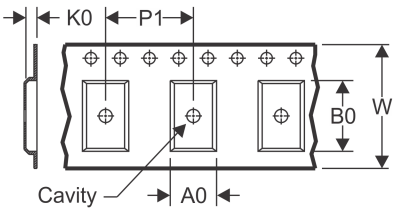
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

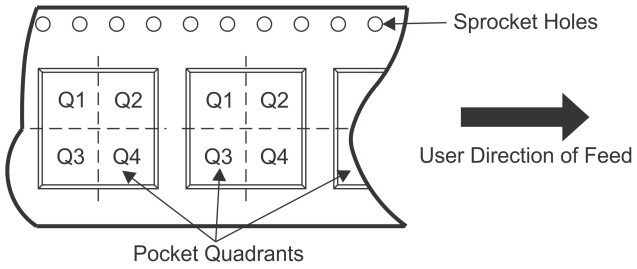


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

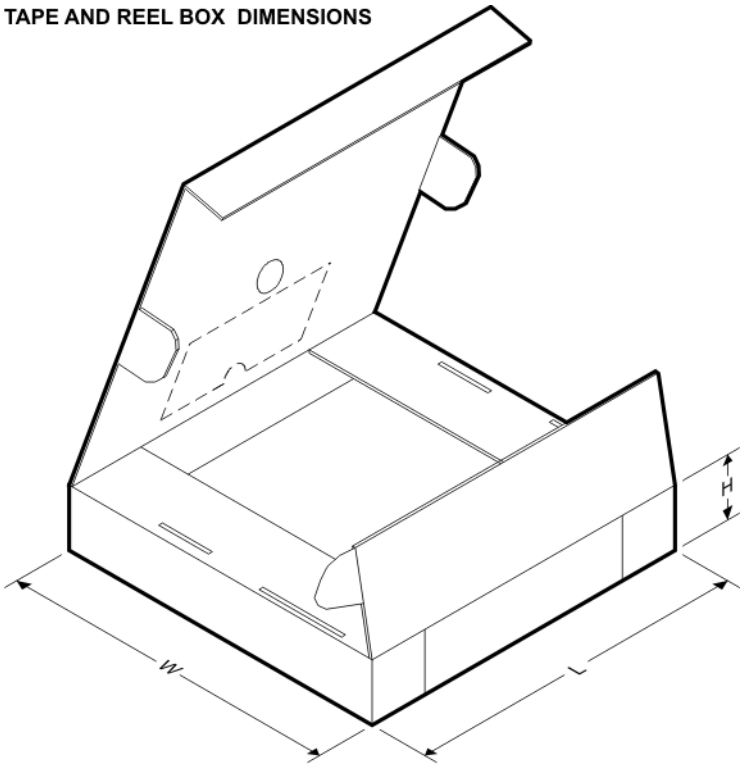


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5951MF-1.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-2.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-1.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-2.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MG-1.3/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-1.5/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5951MG-1.8/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-2.0/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-2.5/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-2.8/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-3.0/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-3.3/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-1.3/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-1.5/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-1.8/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-2.5/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-2.8/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-3.0/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-3.3/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

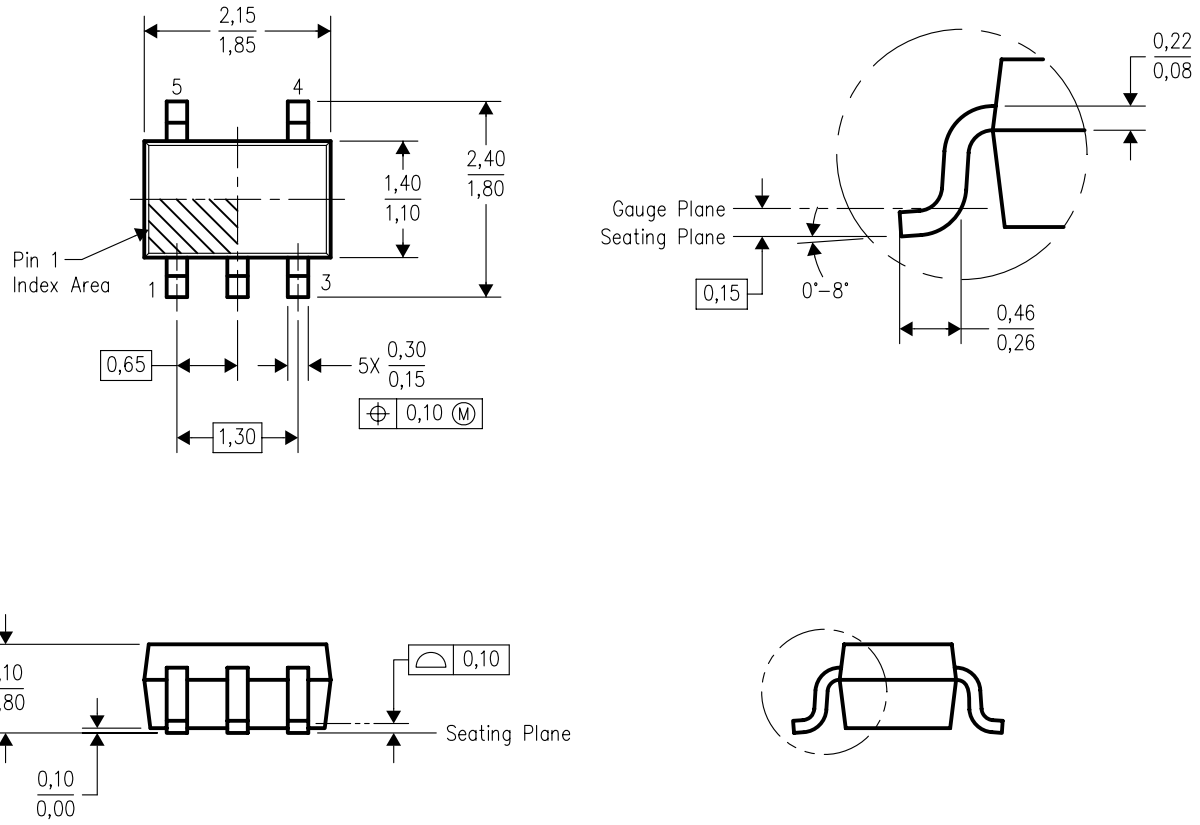


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5951MF-1.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-1.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-2.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5951MF-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MFX-1.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-2.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MG-1.3/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-1.5/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-1.8/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-2.0/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-2.5/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-2.8/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-3.0/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-3.3/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MGX-1.3/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-1.5/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-1.8/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-2.5/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-2.8/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-3.0/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-3.3/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

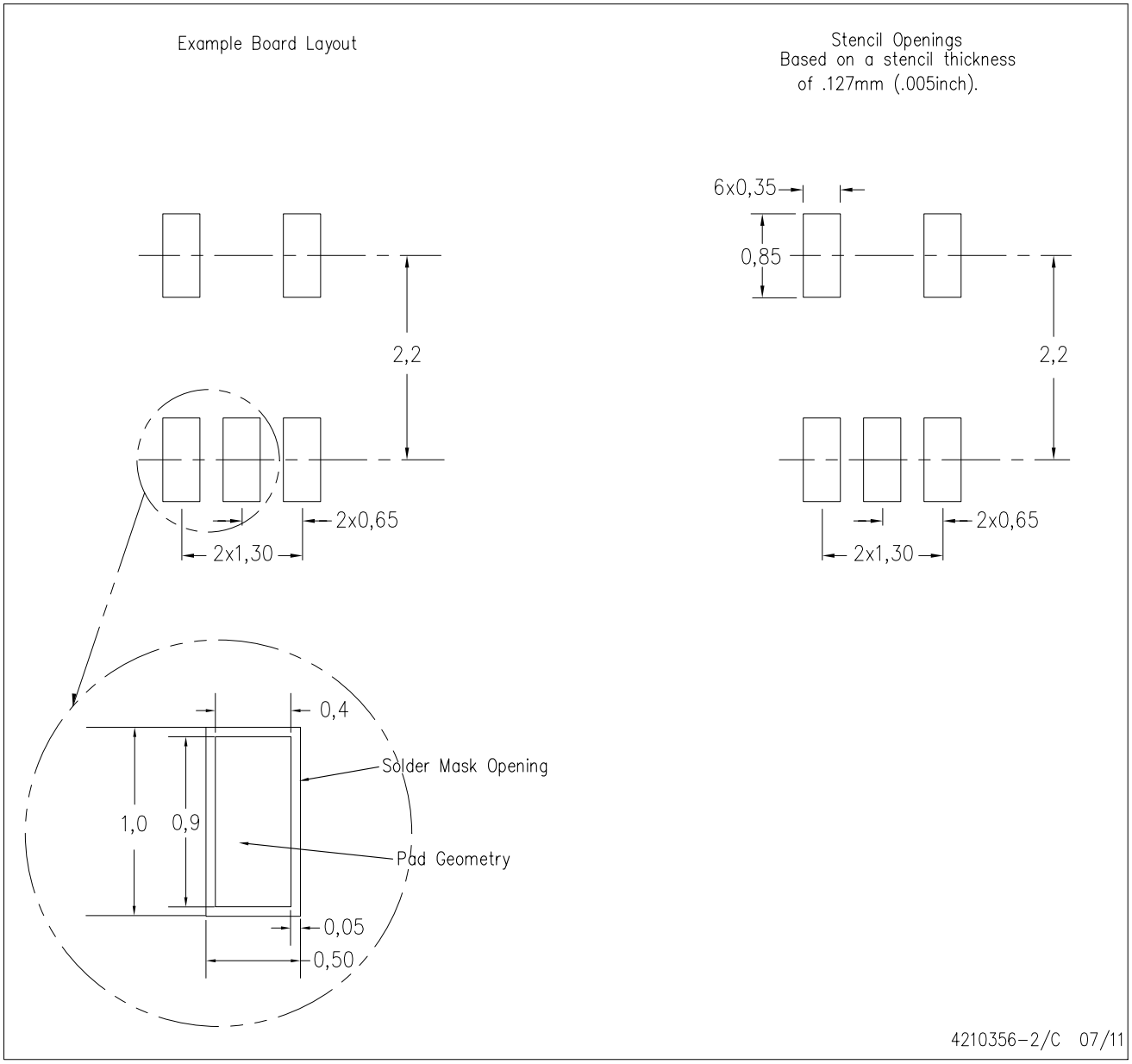
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



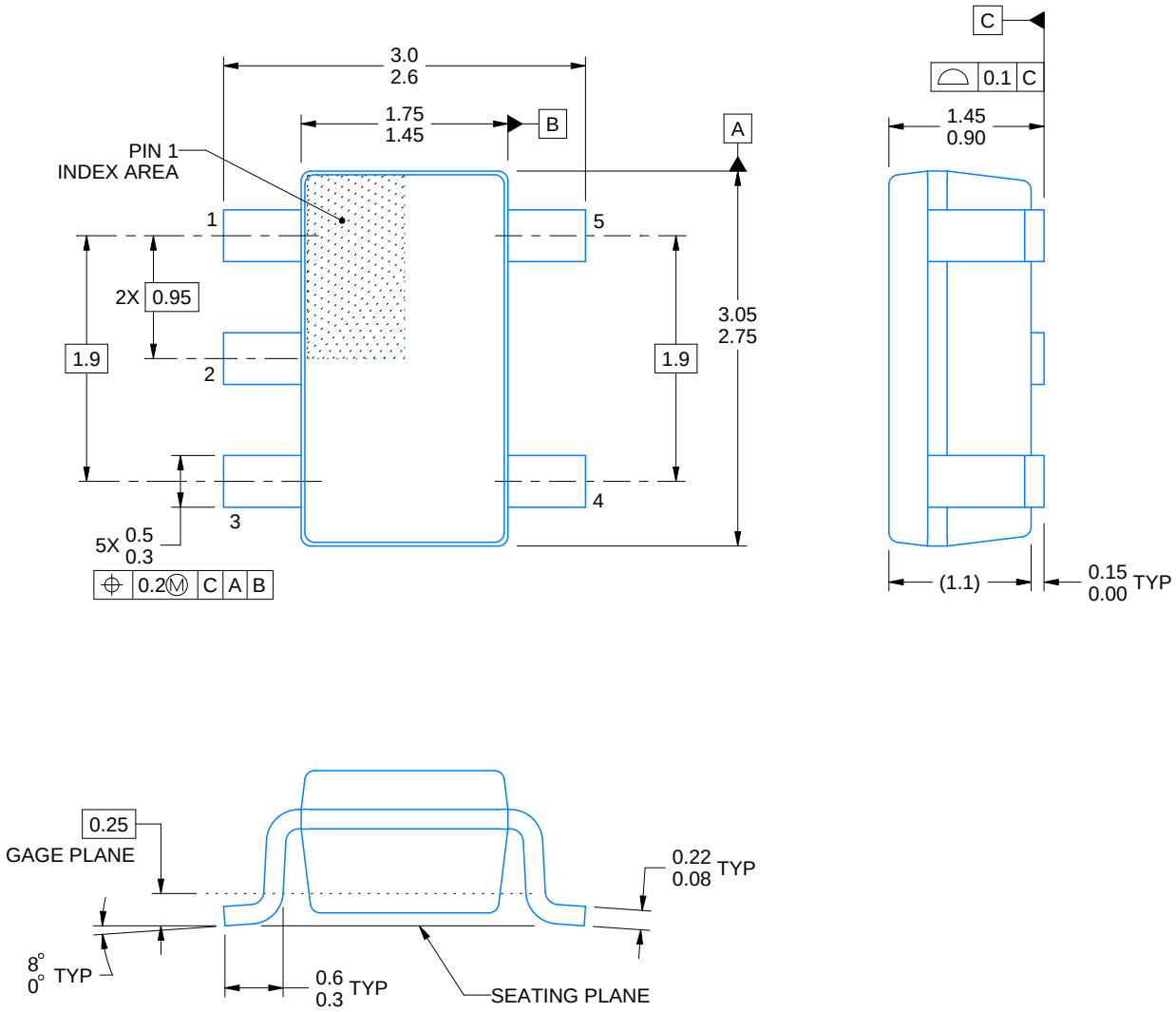
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

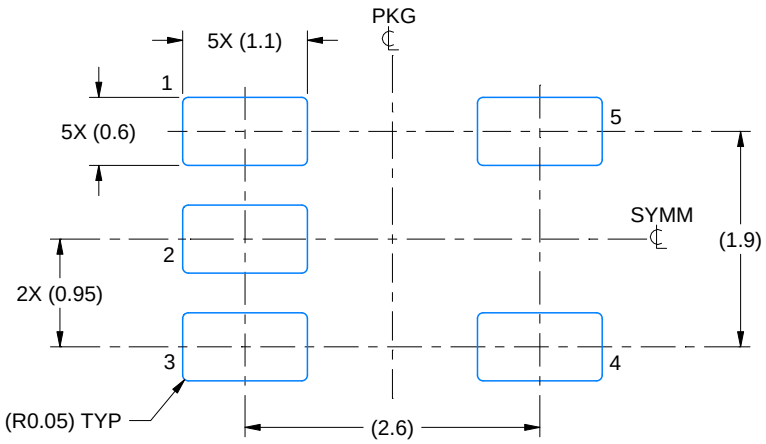
SMALL OUTLINE TRANSISTOR



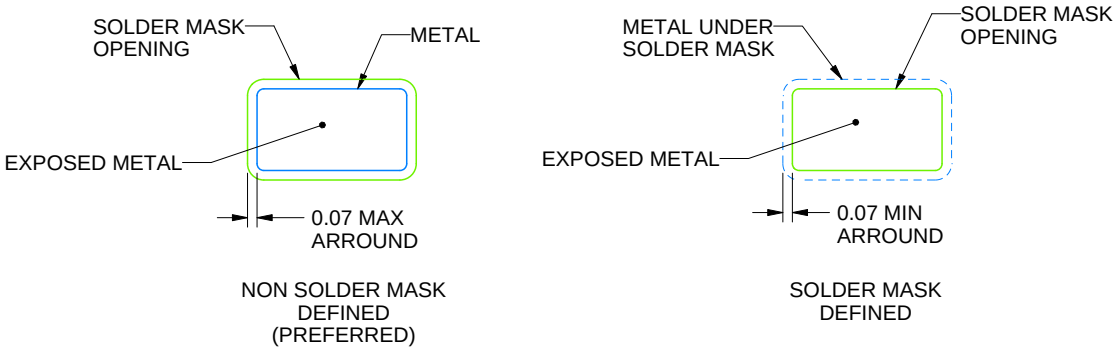
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

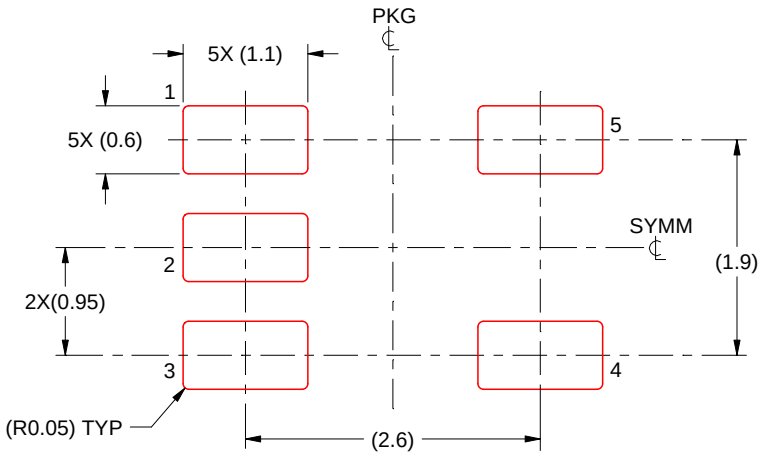


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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