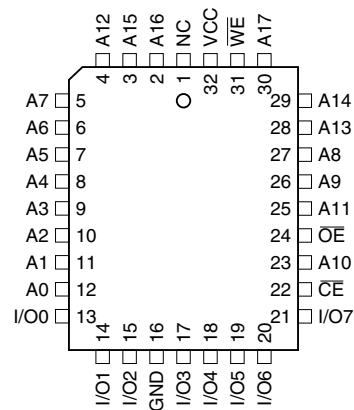


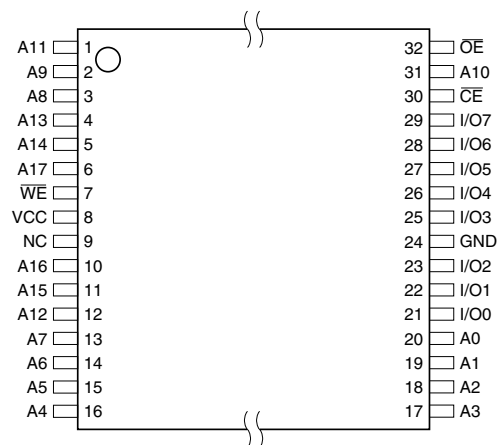
2. Pin Configurations

Pin Name	Function
A0 - A17	Addresses
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
\overline{WE}	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

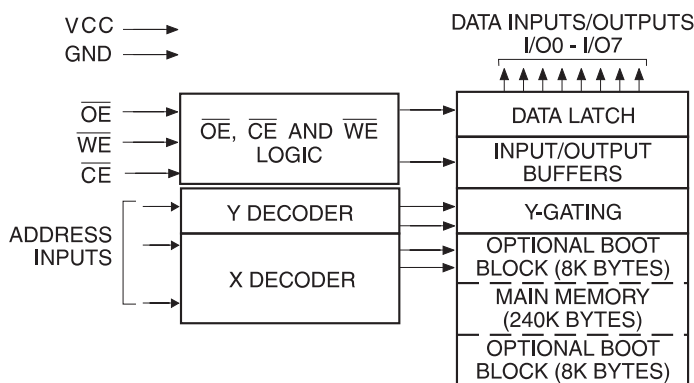
2.1 32-lead PLCC Top View



2.2 32-lead TSOP (Type 1) Top View



3. Block Diagram



4. Device Operation

4.1 Read

The AT29C020 is accessed like an EPROM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention.

4.2 Byte Load

Byte loads are used to enter the 256 bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high. The address is latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} .

4.3 Program

The device is reprogrammed on a sector basis. If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be indeterminate. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high-to-low transition on \overline{WE} (or \overline{CE}) within 150 μ s of the low-to-high transition of \overline{WE} (or \overline{CE}) of the preceding byte. If a high-to-low transition is not detected within 150 μ s of the last low-to-high transition, the load period will end and the internal programming period will start. A8 to A17 specify the sector address. The sector address must be valid during each high-to-low transition of \overline{WE} (or \overline{CE}). A0 to A7 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC} , a read operation will effectively be a polling operation.

4.4 Software Data Protection

A software controlled data protection feature is available on the AT29C020. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when

shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the sector program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature; however, the software feature will guard against inadvertent program cycles during power transitions.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC} , a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a sector of data is loaded into the device using the sector program timing specifications.

4.5 Hardware Data Protection

Hardware features protect against inadvertent programs to the AT29C020 in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8V (typical), the program function is inhibited; (b) V_{CC} power on delay – once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming; (c) Program inhibit – holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits program cycles; and (d) Noise filter – pulses of less than 15 ns (typical) on the \overline{WE} or \overline{CE} inputs will not initiate a program cycle.

4.6 Product Identification

The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

4.7 \overline{DATA} Polling

The AT29C020 features \overline{DATA} polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. \overline{DATA} polling may begin at any time during the program cycle.

4.8 Toggle Bit

In addition to \overline{DATA} polling the AT29C020 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

4.9 Optional Chip Erase Mode

The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

4.10 Boot Block Programming Lockout

The AT29C020 has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 8K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 8K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29C020 blocks are located in the first 8K bytes of memory and the last 8K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

4.10.1 Boot Block Lockout Detection

A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location 3FFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

5. Absolute Maximum Ratings*

Temperature Under Bias.....	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to $V_{CC} + 0.6V$
Voltage on \overline{OE} with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6. DC and AC Operating Range

		AT29C020-70	AT29C020-90	AT29C020-10	AT29C020-12	AT29C020-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V _{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Note: Not recommended for New Designs.

7. Operating Modes

Mode	\overline{CE}	\overline{OE}	\overline{WE}	Ai	I/O
Read	V _{IL}	V _{IL}	V _{IH}	Ai	D _{OUT}
Program ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	Ai	D _{IN}
5V Chip Erase	V _{IL}	V _{IH}	V _{IL}	Ai	
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	X	High Z
Program Inhibit	X	X	V _{IH}		
Program Inhibit	X	V _{IL}	X		
Output Disable	X	V _{IH}	X		High Z
Product Identification					
Hardware	V _{IL}	V _{IL}	V _{IH}	A1 - A17 = V _{IL} , A9 = V _H , ⁽³⁾ A0 = V _{IL}	Manufacturer Code ⁽⁴⁾
				A1 - A17 = V _{IL} , A9 = V _H , A0 = V _{IH}	Device Code ⁽⁴⁾
Software ⁽⁵⁾				A0 = V _{IL}	Manufacturer Code ⁽⁴⁾
				A0 = V _{IH}	Device Code ⁽⁴⁾

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Refer to AC Programming Waveforms.
 3. V_H = 12.0V ± 0.5V.
 4. Manufacturer Code: 1F, Device Code: DA.
 5. See details under Software Product Identification Entry/Exit.

8. DC Characteristics

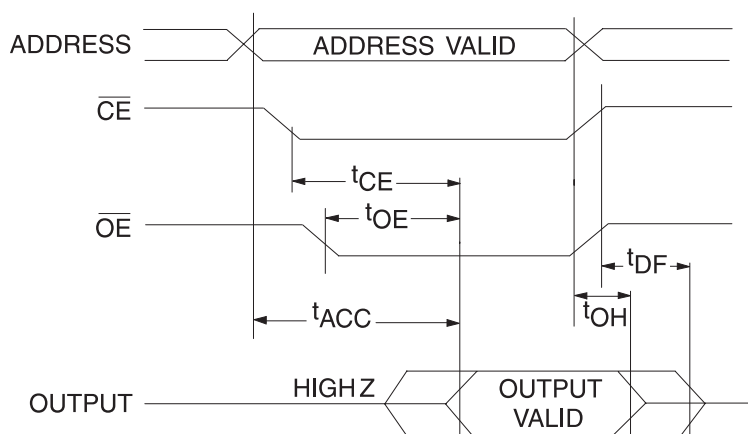
Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC}		10	μA
I _{LO}	Output Leakage Current	V _{I/O} = 0V to V _{CC}		10	μA
I _{SB1}	V _{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V _{CC}	Com.	100	μA
			Ind.	300	μA
I _{SB2}	V _{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to V _{CC}		3	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz; I _{OUT} = 0 mA		40	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.45	V
V _{OH1}	Output High Voltage	I _{OH} = -400 μA	2.4		V
V _{OH2}	Output High Voltage CMOS	I _{OH} = -100 μA; V _{CC} = 4.5V	4.2		V

9. AC Read Characteristics

Symbol	Parameter	AT29C020-90		AT29C020-90		AT29C020-10		AT29C020-12		AT29C020-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	0	70	0	90		100		120		150	ns
$t_{CE}^{(1)}$	\overline{CE} to Output Delay		70		90		100		120		150	ns
$t_{OE}^{(2)}$	\overline{OE} to Output Delay	0	40	0	40	0	50	0	50	0	70	ns
$t_{DF}^{(3)(4)}$	\overline{CE} or \overline{OE} to Output Float	0	25	0	25	0	25	0	30	0	40	ns
t_{OH}	Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first	0		0		0		0		0		ns

Note: Not recommended for New Designs.

10. AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾



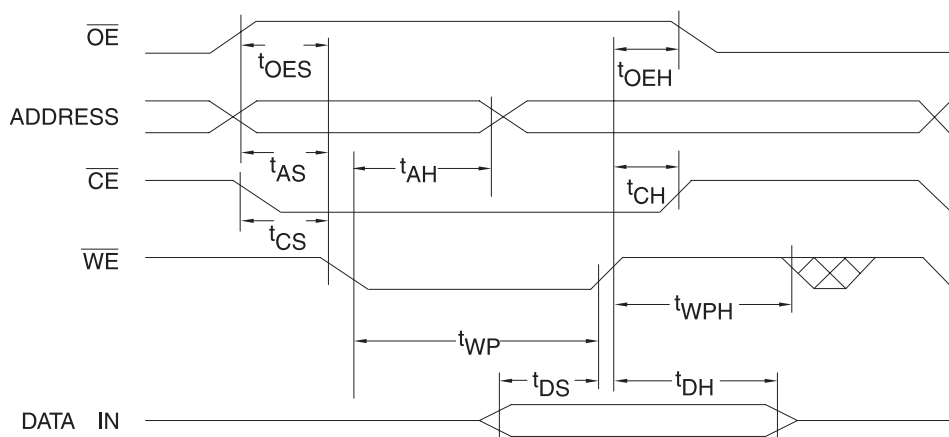
- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first (CL = 5 pF).
 - This parameter is characterized and is not 100% tested.

14. AC Byte Load Characteristics

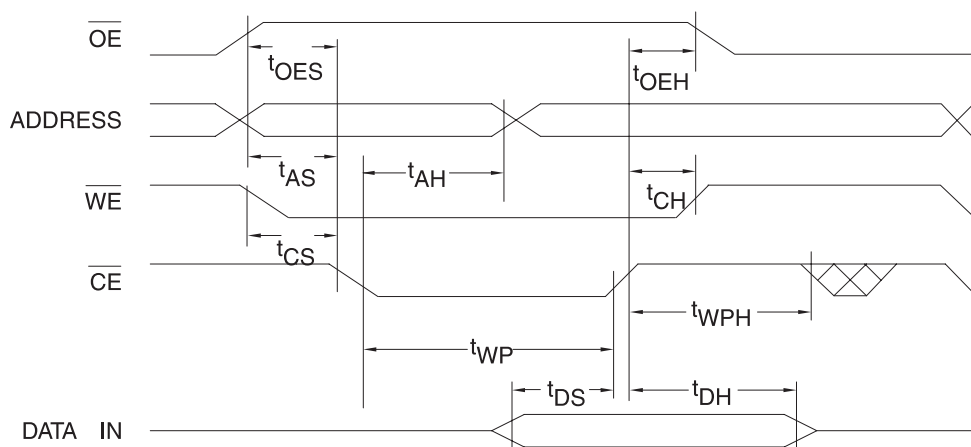
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, \overline{OE} Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width (\overline{WE} or \overline{CE})	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, \overline{OE} Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

15. AC Byte Load Waveforms

15.1 \overline{WE} Controlled



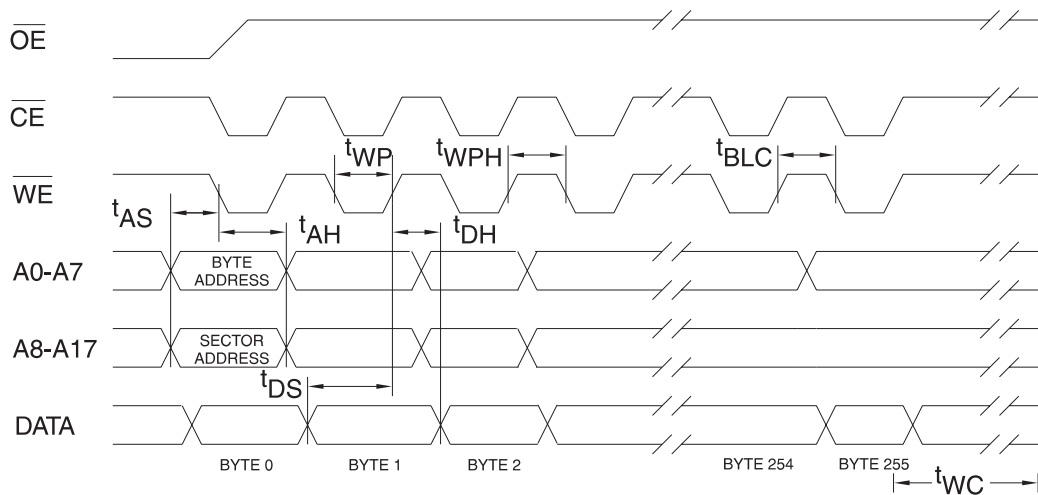
15.2 \overline{CE} Controlled



16. Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	μ s
t_{WPH}	Write Pulse Width High	100		ns

17. Program Cycle Waveforms⁽¹⁾⁽²⁾⁽³⁾



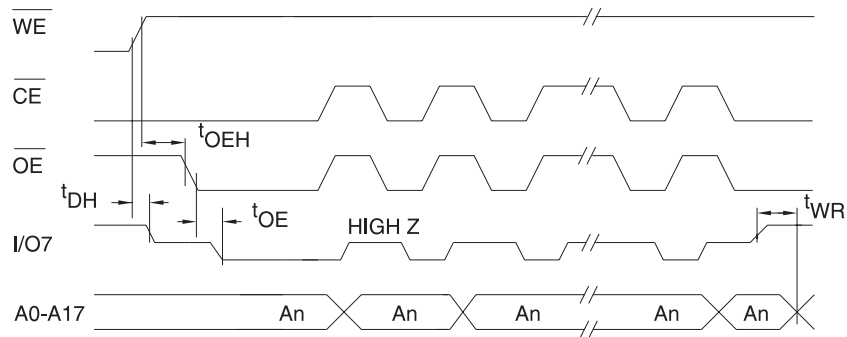
- Notes:
1. A8 through A17 must specify the sector address during each high-to-low transition of \overline{WE} (or \overline{CE}).
 2. \overline{OE} must be high when \overline{WE} and \overline{CE} are both low.
 3. All words that are not loaded within the sector being programmed will be indeterminate.

21. Data Polling Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
$t_{OE\overline{H}}$	\overline{OE} Hold Time	10			ns
t_{OE}	\overline{OE} to Output Delay ⁽²⁾				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

22. Data Polling Waveforms

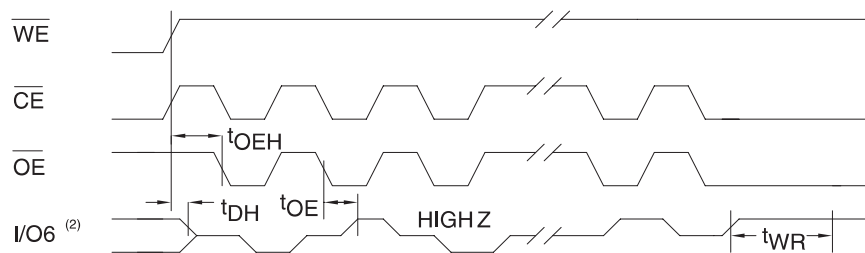


23. Toggle Bit Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
$t_{OE\overline{H}}$	\overline{OE} Hold Time	10			ns
t_{OE}	\overline{OE} to Output Delay ⁽²⁾				ns
t_{OEHP}	\overline{OE} High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

24. Toggle Bit Waveforms⁽¹⁾⁽²⁾⁽³⁾



Notes: 1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.
2. Beginning and ending state of I/O6 may vary.
3. Any address location may be used but the address should not vary.

28. Ordering Information

28.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	40	0.1	AT29C020-70JC AT29C020-70TC	32J 32T	Commercial (0° to 70°C)
	40	0.3	AT29C020-70JI AT29C020-70TI	32J 32T	Industrial (-40° to 85°C)
90	40	0.1	AT29C020-90JC AT29C020-90TC	32J 32T	Commercial (0° to 70°C)
	40	0.3	AT29C020-90JI AT29C020-90TI	32J 32T	Industrial (-40° to 85°C)
100	40	0.1	AT29C020-10JC AT29C020-10TC	32J 32T	Commercial (0° to 70°C)
	40	0.3	AT29C020-10JI AT29C020-10TI	32J 32T	Industrial (-40° to 85°C)
120	40	0.1	AT29C020-12JC AT29C020-12TC	32J 32T	Commercial (0° to 70°C)
	40	0.3	AT29C020-12JI AT29C020-12TI	32J 32T	Industrial (-40° to 85°C)
150	40	0.1	AT29C020-15JC AT29C020-15TC	32J 32T	Commercial (0° to 70°C)
	40	0.3	AT29C020-15JI AT29C020-15TI	32J 32T	Industrial (-40° to 85°C)

Note: Not recommended for New Designs.

28.2 Green Package Option (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	40	0.3	AT29C020-70JU AT29C020-70TU	32J 32T	Industrial (-40° to 85°C)
90	40	0.3	AT29C020-90JU AT29C020-90TU	32J 32T	Commercial (0° to 70°C)

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
32T	32-lead, Thin Small Outline Package (TSOP)