

# 1. Cyclone IV Device Datasheet

CYIV-53001-1.5

This chapter describes the electrical and switching characteristics for Cyclone® IV devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

This chapter includes the following sections:

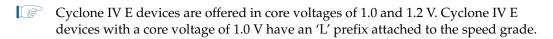
- "Operating Conditions" on page 1–1
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## **Operating Conditions**

When Cyclone IV devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone IV devices, you must consider the operating requirements described in this chapter.

Cyclone IV devices are offered in commercial, industrial, extended industrial and, automotive grades. Cyclone IV E devices offer –6 (fastest), –7, –8, –8L, and –9L speed grades for commercial devices, –8L speed grades for industrial devices, and –7 speed grade for extended industrial and automotive devices. Cyclone IV GX devices offer –6 (fastest), –7, and –8 speed grades for commercial devices and –7 speed grade for industrial devices.





In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with a "C" prefix, industrial with an "I" prefix, and automotive with an "A" prefix. Therefore, commercial devices are indicated as C6, C7, C8, C8L, or C9L per respective speed grade. Industrial devices are indicated as I7, I8, or I8L. Automotive devices are indicated as A7.

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Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

## **Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.



Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices (1) — Preliminary

Symbol	Parameter	Min	Max	Unit
V <sub>CCINT</sub>	Core voltage, PCI Express® (PCIe®) hard IP block, and transceiver physical coding sublayer (PCS) power supply	-0.5	1.8	V
V <sub>CCA</sub>	Phase-locked loop (PLL) analog power supply	-0.5	3.75	V
V <sub>CCD_PLL</sub>	PLL digital power supply	-0.5	1.8	V
V <sub>CCIO</sub>	I/O banks power supply	-0.5	3.9	V
V <sub>CC_CLKIN</sub>	Differential clock input pins power supply	-0.5	3.9	V
V <sub>CCH_GXB</sub>	Transceiver output buffer power supply	-0.5	2.625	V
V <sub>CCA_GXB</sub>	Transceiver physical medium attachment (PMA) and auxiliary power supply	-0.5	2.625	V
V <sub>CCL_GXB</sub>	Transceiver PMA and auxiliary power supply	-0.5	1.8	V
VI	DC input voltage	-0.5	3.95	V
I <sub>OUT</sub>	DC output current, per pin	-25	40	mA
T <sub>STG</sub>	Storage temperature	-65	150	°C
T <sub>J</sub>	Operating junction temperature	-40	125	°C

#### Note to Table 1-1:

## **Maximum Allowed Overshoot or Undershoot Voltage**

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to -2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1-2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

<sup>(1)</sup> Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.



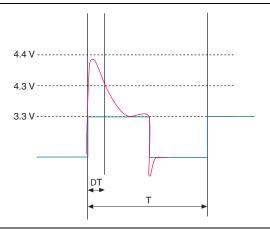
A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3~V can only be at 4.3~V for 65% over the lifetime of the device; for a device lifetime of 10~V years, this amounts to 65/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
		V <sub>I</sub> = 4.20	100	%
		V <sub>I</sub> = 4.25	98	%
		V <sub>I</sub> = 4.30	65	%
		V <sub>I</sub> = 4.35	43	%
V <sub>i</sub>	AC Input Voltage	V <sub>I</sub> = 4.40	29	%
	Voltago	V <sub>I</sub> = 4.45	20	%
		V <sub>I</sub> = 4.50	13	%
		V <sub>I</sub> = 4.55	9	%
		V <sub>I</sub> = 4.60	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as ([delta T]/T)  $\times$  100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1-1. Cyclone IV Devices Overshoot Duration



## **Recommended Operating Conditions**

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices (1), (2) (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CCINT</sub> (3)	Supply voltage for internal logic, 1.2-V operation	_	1.15	1.2	1.25	V
VCCINT 17	Supply voltage for internal logic, 1.0-V operation	_	0.97	1.0	1.03	V
	Supply voltage for output buffers, 3.3-V operation	_	3.135	3.3	3.465	V
	Supply voltage for output buffers, 3.0-V operation	_	2.85	3	3.15	V
V <sub>CCIO</sub> (3), (4)	Supply voltage for output buffers, 2.5-V operation	_	2.375	2.5	2.625	V
VCCIO V	Supply voltage for output buffers, 1.8-V operation	_	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	_	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	_	1.14	1.2	1.26	V
V <sub>CCA</sub> (3)	Supply (analog) voltage for PLL regulator	_	2.375	2.5	2.625	V
V (3)	Supply (digital) voltage for PLL, 1.2-V operation	_	1.15	1.2	1.25	V
V <sub>CCD_PLL</sub> (3)	Supply (digital) voltage for PLL, 1.0-V operation	_	0.97	1.0	1.03	V
V <sub>I</sub>	Input voltage	_	-0.5	_	3.6	V
V <sub>0</sub>	Output voltage	_	0	_	V <sub>CCIO</sub>	V
		For commercial use	0	_	85	°C
_	Operating junction temperature	For industrial use	-40	_	100	°C
T <sub>J</sub>	Operating junction temperature	For extended temperature (5)	-40	_	125	°C
		For automotive use	-40	_	125	°C
t <sub>RAMP</sub>	Power supply ramp time	Standard power-on reset (POR) (6)	50 μs	_	50 ms	_
	·	Fast POR (7)	50 μs	_	3 ms	_

Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices (1), (2) (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I <sub>Diode</sub>	Magnitude of DC current across PCI-clamp diode when enable	-	_	_	10	mA

#### Notes to Table 1-3:

- (1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades.
- (2) V<sub>CCIO</sub> for all I/O banks must be powered up during device operation. All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (3)  $V_{CC}$  must rise monotonically.
- (4)  $V_{CCIO}$  powers all input buffers.
- (5) The I7 devices support extended operating junction temperature up to 125°C (usual range is -40°C to 100°C). When using I7 devices at the extended junction temperature ranging from -40°C to 125°C, select C8 as the target device when designing in the Quartus® II software. The I7 devices meet all C8 timing specifications when I7 devices operate beyond 100°C and up to 125°C.
- (6) The POR time for Standard POR ranges between 50 and 200 ms. Each individual power supply must reach the recommended operating range within 50 ms.
- (7) The POR time for Fast POR ranges between 3 and 9 ms. Each individual power supply must reach the recommended operating range within 3 ms.

Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 1 of 2)—Preliminary

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CCINT</sub> (3)	Core voltage, PCIe hard IP block, and transceiver PCS power supply	_	1.16	1.2	1.24	V
V <sub>CCA</sub> (1), (3)	PLL analog power supply	_	2.375	2.5	2.625	V
V <sub>CCD_PLL</sub> (2)	PLL digital power supply	_	1.16	1.2	1.24	V
	I/O banks power supply for 3.3-V operation	_	3.135	3.3	3.465	V
	I/O banks power supply for 3.0-V operation	_	2.85	3	3.15	V
V (3), (4)	I/O banks power supply for 2.5-V operation	_	2.375	2.5	2.625	V
V <sub>CCIO</sub> (3), (4)	I/O banks power supply for 1.8-V operation	_	1.71	1.8	1.89	V
	I/O banks power supply for 1.5-V operation	_	1.425	1.5	1.575	V
	I/O banks power supply for 1.2-V operation	_	1.14	1.2	1.26	V
	Differential clock input pins power supply for 3.3-V operation	_	3.135	3.3	3.465	V
	Differential clock input pins power supply for 3.0-V operation	_	2.85	3	3.15	V
V <sub>CC_CLKIN</sub>	Differential clock input pins power supply for 2.5-V operation	_	2.375	2.5	2.625	V
(3), (5), (6)	Differential clock input pins power supply for 1.8-V operation	_	1.71	1.8	1.89	V
	Differential clock input pins power supply for 1.5-V operation	_	1.425	1.5	1.575	V
	Differential clock input pins power supply for 1.2-V operation	_	1.14	1.2	1.26	V

Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)—Preliminary

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CCH_GXB</sub>	Transceiver output buffer power supply	_	2.375	2.5	2.625	V
V <sub>CCA_GXB</sub>	Transceiver PMA and auxiliary power supply	_	2.375	2.5	2.625	V
V <sub>CCL_GXB</sub>	Transceiver PMA and auxiliary power supply	_	1.16	1.2	1.24	V
V <sub>I</sub>	DC input voltage	_	-0.5	_	3.6	V
V <sub>0</sub>	DC output voltage	_	0	_	V <sub>CCIO</sub>	V
TJ	Operating junction temperature	For commercial use	0		85	°C
IJ	Operating junction temperature	For industrial use	-40	_	100	°C
t <sub>RAMP</sub>	Power supply ramp time	Standard power-on reset (POR) (7)	50 μs	_	50 ms	_
TUZNINI		Fast POR (8)	50 μs	_	3 ms	_
I <sub>Diode</sub>	Magnitude of DC current across PCI-clamp diode when enabled	_	_	_	10	mA

#### Notes to Table 1-4:

- (1) All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (2) You must connect  $V_{CCD\ PLL}$  to  $V_{CCINT}$  through a decoupling capacitor and ferrite bead.
- (3) Power supplies must rise monotonically.
- (4) V<sub>CCIO</sub> for all I/O banks must be powered up during device operation. Configurations pins are powered up by V<sub>CCIO</sub> of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V<sub>CCIO</sub> of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V<sub>CCIO</sub> level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- (5) You must set  $V_{\text{CC\_CLKIN}}$  to 2.5 V if you use CLKIN as a high-speed serial interface (HSSI) refclk or as a DIFFCLK input.
- (6) The CLKIN pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- (7) The POR time for Standard POR ranges between 50 and 200 ms. V<sub>CCINT</sub>, V<sub>CCA</sub>, and V<sub>CCIO</sub> of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- (8) The POR time for Fast POR ranges between 3 and 9 ms. V<sub>CCINT</sub>, V<sub>CCA</sub>, and V<sub>CCIO</sub> of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

#### **ESD Performance**

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1–5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V	ESD voltage using the HBM (GPIOs) (1)	± 2000	V
VESDHBM	ESD using the HBM (HSSI I/Os) (2)	± 1000	V
V <sub>ESDCDM</sub>	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) (2)	± 250	V

#### Notes to Table 1-5:

- (1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ±1000V.
- (2) This value is applicable only to Cyclone IV GX devices.

### **DC** Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

## **Supply Current**

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1–6 lists the I/O pin leakage current for Cyclone IV devices.

Table 1–6. I/O Pin Leakage Current for Cyclone IV Devices (1), (2)

Symbol	Parameter	Conditions	Device	Min	Тур	Max	Unit
I <sub>I</sub>	Input pin leakage current	$V_I = 0 V \text{ to } V_{CCIOMAX}$		-10	_	10	μΑ
I <sub>OZ</sub>	Tristated I/O pin leakage current	$V_0 = 0 \text{ V to } V_{\text{CCIOMAX}}$		-10	_	10	μΑ

#### Notes to Table 1-6:

- (1) This value is specified for normal device operation. The value varies during device power-up. This applies for all V<sub>CCIO</sub> settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).
- (2) The 10  $\mu$ A I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

#### **Bus Hold**

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–7 lists bus hold specifications for Cyclone IV devices.

Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2) (1)—Preliminary

				V <sub>CCIO</sub> (V)										
Parameter	Condition	1.2		1.5		1.8		2.5		3.0		3.3		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold low, sustaining current	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	8	_	12	_	30	_	50	_	70	_	70	_	μА
Bus hold high, sustaining current	V <sub>IN</sub> < V <sub>IL</sub> (minimum)	-8	_	-12	_	-30	_	-50	_	-70	_	-70	_	μА
Bus hold low, overdrive current	0 V < V <sub>IN</sub> < V <sub>CCIO</sub>	_	125	_	175	_	200	_	300	_	500	_	500	μА
Bus hold high, overdrive current	0 V < V <sub>IN</sub> < V <sub>CCIO</sub>	_	-125	_	-175	_	-200	_	-300	—	-500	—	-500	μА

Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 2 of 2) (1)—Preliminary

Parameter		V <sub>CCIO</sub> (V)												
	Condition	1.2		1	1.5		1.8 2		2.5		.0	3.3		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold trip point	_	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

#### Note to Table 1-7:

(1) Bus hold trip points are based on the calculated input voltages from the JEDEC standard.

### **OCT Specifications**

Table 1–8 lists the variation of OCT without calibration across process, temperature, and voltage (PVT).

Table 1-8. Series OCT Without Calibration Specifications for Cyclone IV Devices—Preliminary

		Resistance		
Description	V <sub>CCIO</sub> (V)	Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	Unit
	3.0	±30	±40	%
Onder OOT oddered	2.5	±30	±40	%
Series OCT without calibration	1.8	±40	±50	%
Canbration	1.5	±50	±50	%
	1.2	±50	±50	%

OCT calibration is automatically performed at device power-up for OCT-enabled I/Os.

Table 1–9 lists the OCT calibration accuracy at device power-up.

Table 1–9. Series OCT with Calibration at Device Power-Up Specifications for Cyclone IV Devices
—Preliminary

		Calibratio		
Description	V <sub>CCIO</sub> (V)	Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	Unit
	3.0	±10	±10	%
Series OCT with	2.5	±10	±10	%
calibration at device	1.8	±10	±10	%
power-up	1.5	±10	±10	%
	1.2	±10	±10	%

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up. Use Table 1–10 and Equation 1–1 to determine the final OCT resistance considering the variations after calibration at device power-up. Table 1–10 lists the change percentage of the OCT resistance with voltage and temperature.

Table 1–10. OCT Variation After Calibration at Device Power-Up for Cyclone IV Devices— Preliminary

Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
3.0	0.262	-0.026
2.5	0.234	-0.039
1.8	0.219	-0.086
1.5	0.199	-0.136
1.2	0.161	-0.288

## Equation 1-1. Final OCT Resistance (1), (2), (3), (4), (5), (6)

#### Notes to Equation 1-1:

- (1) T<sub>2</sub> is the final temperature.
- (2)  $T_1$  is the initial temperature.
- (3) MF is multiplication factor.
- (4) R<sub>final</sub> is final resistance.
- (5) R<sub>initial</sub> is initial resistance.
- (6) Subscript  $_x$  refers to both  $_V$  and  $_T$ .
- (7)  $\Delta R_V$  is a variation of resistance with voltage.
- (8)  $\Delta R_T$  is a variation of resistance with temperature.
- (9) dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
- (10) dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
- (11) V<sub>2</sub> is final voltage.
- (12)  $V_1$  is the initial voltage.

Operating Conditions

Example 1–1 shows how to calculate the change of 50- $\Omega$  I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

### Example 1-1. Impedance Change

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$

$$\Delta R_T = (85 - 25) \times 0.262 = 15.72$$

Because  $\Delta R_V$  is negative,

$$MF_V = 1 / (3.83/100 + 1) = 0.963$$

Because  $\Delta R_T$  is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{final} = 50 \times 1.114 = 55.71 \Omega$$

## **Pin Capacitance**

Table 1–11 lists the pin capacitance for Cyclone IV devices.

Table 1-11. Pin Capacitance for Cyclone IV Devices —Preliminary

Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Quad Flat No Leads (QFN)	Typical – Fineline BGA (FBGA)	Unit
$C_{IOTB}$	Input capacitance on top and bottom I/O pins	7	7	6	pF
C <sub>IOLR</sub>	Input capacitance on right I/O pins	7	7	5	pF
C <sub>LVDSLR</sub>	Input capacitance on right I/O pins with dedicated LVDS output	8	8	7	pF
C <sub>VREFLR</sub>	Input capacitance on right dual-purpose $\ensuremath{VREF}$ pin when used as $V_{REF}$ or user I/O pin	21	21	21	pF
C <sub>VREFTB</sub>	Input capacitance on top and bottom dual-purpose ${\tt VREF}$ pin when used as $V_{REF}$ or user I/O pin	23 (2)	23	23	pF
C <sub>CLKTB</sub>	Input capacitance on top and bottom dedicated clock input pins	7	7	6	pF
C <sub>CLKLR</sub>	Input capacitance on right dedicated clock input pins	6	6	5	pF

#### Notes to Table 1-11:

- (1) When you use the VREF pin as a regular input or output, you can expect a reduced performance of toggle rate and  $t_{CO}$  because of higher pin capacitance.
- (2)  $C_{VREFTB}$  for the EP4CE22 device is 30 pF.

### Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1-12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

Table 1–12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices (1) —Preliminary

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_{CCIO} = 3.3 \text{ V} \pm 5\%$ (2), (3)	7	25	41	kΩ
	alue of the I/O pin pull-up resistor	$V_{CCIO} = 3.0 \text{ V} \pm 5\%$ (2), (3)	7	28	47	kΩ
<b>D</b>	before and during configuration, as	$V_{CCIO} = 2.5 \text{ V} \pm 5\%$ (2), (3)	8	35	61	kΩ
R_ <sub>PU</sub>	well as user mode if you enable the	$V_{CCIO} = 1.8 \text{ V} \pm 5\%$ (2), (3)	10	57	108	kΩ
	programmable pull-up resistor option	$V_{CCIO} = 1.5 \text{ V} \pm 5\%$ (2), (3)	13	82	163	kΩ
		$V_{CCIO} = 1.2 \text{ V} \pm 5\%$ (2), (3)	19	143	351	kΩ
		$V_{CCIO} = 3.3 \text{ V} \pm 5\%$ (4)	6	19	30	kΩ
	Value of the I/O min mult down was into	$V_{CCIO} = 3.0 \text{ V} \pm 5\%$ (4)	6	22	36	kΩ
R_PD	Value of the I/O pin pull-down resistor before and during configuration	$V_{CCIO} = 2.5 \text{ V} \pm 5\%$ (4)	6	25	43	kΩ
	Soloto and dailing configuration	$V_{CCIO} = 1.8 \text{ V} \pm 5\%$ (4)	7	35	71	kΩ
		$V_{CCIO} = 1.5 \text{ V} \pm 5\%$ (4)	8	50	112	kΩ

#### Notes to Table 1-12:

- (1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V<sub>CCIO</sub>.
- (3)  $R_{PU} = (V_{CC10} V_1)/I_{R_PU}$ Minimum condition:  $-40^{\circ}C$ ;  $V_{CC10} = V_{CC} + 5\%$ ,  $V_1 = V_{CC} + 5\% 50$  mV; Typical condition:  $25^{\circ}C$ ;  $V_{CC10} = V_{CC}$ ,  $V_1 = 0$  V;  $V_2 = 0$  V;  $V_3 = 0$  V;  $V_4 = 0$  V and  $V_5 = 0$  V and  $V_6 = 0$  V and  $V_7 = 0$  V and  $V_8 = 0$  V and  $V_$ 

  - Maximum condition:  $100^{\circ}\text{C}$ ;  $V_{\text{CCIO}} = V_{\text{CC}} 5\%$ ,  $V_{\text{I}} = 0$  V; in which  $V_{\text{I}}$  refers to the input voltage at the I/O pin.
- (4)  $R_{PD} = V_I/I_{RPD}$ 
  - Minimum condition: -40°C;  $V_{CCIO} = V_{CC} + 5\%$ ,  $V_I = 50$  mV;

  - Typical condition: 25°C;  $V_{CCIO} = V_{CC}$ ,  $V_1 = V_{CC} 5\%$ ; Maximum condition: 100°C;  $V_{CCIO} = V_{CC} 5\%$ ,  $V_1 = V_{CC} 5\%$ ; in which  $V_1$  refers to the input voltage at the I/O pin.

### **Hot-Socketing**

Table 1–13 lists the hot-socketing specifications for Cyclone IV devices.

Table 1–13. Hot-Socketing Specifications for Cyclone IV Devices —Preliminary

Symbol	Parameter	Maximum
I <sub>IOPIN(DC)</sub>	DC current per I/O pin	300 μΑ
I <sub>IOPIN(AC)</sub>	AC current per I/O pin	8 mA (1)
I <sub>XCVRTX(DC)</sub>	DC current per transceiver TX pin	100 mA
I <sub>XCVRRX(DC)</sub>	DC current per transceiver RX pin	50 mA

#### Note to Table 1-13:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.



During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

## Schmitt Trigger Input

Cyclone IV devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF\_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate. Table 1-14 lists the hysteresis specifications across the supported  $V_{\rm CCIO}$  range for Schmitt trigger inputs in Cyclone IV devices.

Table 1–14. Hysteresis Specifications for Schmitt Trigger Input in Cyclone IV Devices—Preliminary

Symbol	Parameter	Conditions (V)	Minimum	Unit
		$V_{CCIO} = 3.3$	200	mV
V <sub>SCHMITT</sub>	Hysteresis for Schmitt trigger	V <sub>CCIO</sub> = 2.5	200	mV
	input	V <sub>CCIO</sub> = 1.8	140	mV
		V <sub>CCIO</sub> = 1.5	110	mV

## I/O Standard Specifications

The following tables list input voltage sensitivities ( $V_{IH}$  and  $V_{IL}$ ), output voltage ( $V_{OH}$  and  $V_{OL}$ ), and current drive characteristics ( $I_{OH}$  and  $I_{OL}$ ), for various I/O standards supported by Cyclone IV devices. Table 1–15 through Table 1–20 provide the I/O standard specifications for Cyclone IV devices.

Table 1–15. Single-Ended I/O Standard Specifications for Cyclone IV Devices (1). (2) —Preliminary

•			-		-	_		_			
I/O Standard		V <sub>CCIO</sub> (V	)	V	<sub>L</sub> (V)	V	/ <sub>IH</sub> (V)	V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub>	I <sub>OH</sub>
I/O Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
3.3-V LVTTL (3)	3.135	3.3	3.465	_	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS (3)	3.135	3.3	3.465	_	0.8	1.7	3.6	0.2	V <sub>CCIO</sub> - 0.2	2	-2
3.0-V LVTTL (3)	2.85	3.0	3.15	-0.3	0.8	1.7	V <sub>CCIO</sub> + 0.3	0.45	2.4	4	-4
3.0-V LVCMOS (3)	2.85	3.0	3.15	-0.3	0.8	1.7	V <sub>CCIO</sub> + 0.3	0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
2.5 V <sup>(3)</sup>	2.375	2.5	2.625	-0.3	0.7	1.7	V <sub>CCIO</sub> + 0.3	0.4	2.0	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	2.25	0.45	V <sub>CCIO</sub> – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.25 x V <sub>CCIO</sub>	0.75 x V <sub>CCIO</sub>	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 x V <sub>CCIO</sub>	0.65 x V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.25 x V <sub>CCIO</sub>	0.75 x V <sub>CCIO</sub>	2	-2
3.0-V PCI	2.85	3.0	3.15	_	0.3 x V <sub>CCIO</sub>	0.5 x V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.1 x V <sub>CCIO</sub>	0.9 x V <sub>CCIO</sub>	1.5	-0.5
3.0-V PCI-X	2.85	3.0	3.15	_	0.35 x V <sub>CCIO</sub>	0.5 x V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.1 x V <sub>CCIO</sub>	0.9 x V <sub>CCIO</sub>	1.5	-0.5

#### Notes to Table 1-15:

<sup>(1)</sup> For voltage-referenced receiver input waveform and explanation of terms used in Table 1-15, refer to "Glossary" on page 1-38.

<sup>(2)</sup> AC load CL = 10 pF

<sup>(3)</sup> For more information about interfacing Cyclone IV devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards, refer to AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems.

Table 1–16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices (1)
—Preliminary

1/0					V <sub>REF</sub> (V)		V <sub>TT</sub> (V) <sup>(2)</sup>			
Standard	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95	
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79	
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 x V <sub>CCIO</sub> (3) 0.47 x V <sub>CCIO</sub> (4)	0.5 x V <sub>CCIO</sub> (3) 0.5 x V <sub>CCIO</sub> (4)	0.52 x V <sub>CCIO</sub> (3) 0.53 x V <sub>CCIO</sub> (4)	_	0.5 x V <sub>CCIO</sub>	_	

#### Notes to Table 1-16:

- (1) For an explanation of terms used in Table 1–16, refer to "Glossary" on page 1–38.
- (2)  $V_{TT}$  of the transmitting device must track  $V_{REF}$  of the receiving device.
- (3) Value shown refers to DC input reference voltage,  $V_{REF(DC)}$ .
- (4) Value shown refers to AC input reference voltage,  $V_{REF(AC)}$ .

Table 1-17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices—Preliminary

1/0	V <sub>IL(</sub>	<sub>DC)</sub> (V)	VIH	<sub>I(DC)</sub> (V)	V <sub>IL(</sub>	<sub>AC)</sub> (V)	V <sub>IH</sub>	<sub>(AC)</sub> (V)	V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub>	I <sub>OH</sub>
Standard	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min	(mĀ)	(mÄ)
SSTL-2 Class I	_	V <sub>REF</sub> – 0.18	V <sub>REF</sub> + 0.18	_	_	V <sub>REF</sub> – 0.35	V <sub>REF</sub> + 0.35	_	V <sub>π</sub> – 0.57	V <sub>TT</sub> + 0.57	8.1	-8.1
SSTL-2 Class II	_	V <sub>REF</sub> – 0.18	V <sub>REF</sub> + 0.18	_	_	V <sub>REF</sub> – 0.35	V <sub>REF</sub> + 0.35	_	V <sub>TT</sub> – 0.76	V <sub>TT</sub> + 0.76	16.4	-16.4
SSTL-18 Class I	_	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	_	_	V <sub>REF</sub> – 0.25	V <sub>REF</sub> + 0.25	_	V <sub>TT</sub> – 0.475	V <sub>TT</sub> + 0.475	6.7	-6.7
SSTL-18 Class II	_	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	_	_	V <sub>REF</sub> – 0.25	V <sub>REF</sub> + 0.25	_	0.28	V <sub>CCIO</sub> - 0.28	13.4	-13.4
HSTL-18 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	_	V <sub>REF</sub> – 0.2	V <sub>REF</sub> + 0.2	_	0.4	V <sub>CCIO</sub> – 0.4	8	-8
HSTL-18 Class II		V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	_	V <sub>REF</sub> – 0.2	V <sub>REF</sub> + 0.2	_	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	_	V <sub>REF</sub> – 0.2	V <sub>REF</sub> + 0.2	_	0.4	V <sub>CCIO</sub> - 0.4	8	-8
HSTL-15 Class II		V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_		V <sub>REF</sub> – 0.2	V <sub>REF</sub> + 0.2	_	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> – 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	-0.24	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	V <sub>CCIO</sub> + 0.24	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> – 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	-0.24	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	V <sub>CCIO</sub> + 0.24	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	14	-14



For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the I/O Features in Cyclone IV Devices chapter.

Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices (1)—Preliminary

I/O Standard	$\begin{array}{c c} V_{CCIO}(V) & V_{Swing(DC)}(\\ \end{array}$		<sub>I(DC)</sub> (V)	V <sub>x(</sub> ,	<sub>AC)</sub> (V)		V <sub>Swir</sub>	ng(AC) <b>/</b> )	V <sub>OX(AC)</sub> (V)				
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V <sub>CCIO</sub>	V <sub>CCIO</sub> /2 - 0.2	_	V <sub>CCIO</sub> /2 + 0.2	0.7	V <sub>CCI</sub>	V <sub>CCIO</sub> /2 - 0.125	_	V <sub>CCIO</sub> /2 + 0.125
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V <sub>CCIO</sub>	V <sub>CCIO</sub> /2 - 0.175	_	V <sub>CCIO</sub> /2 + 0.175	0.5	V <sub>CCI</sub>	V <sub>CCIO</sub> /2 - 0.125	_	V <sub>CCIO</sub> /2 + 0.125

Note to Table 1-18:

Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices (1)—Preliminary

	V <sub>CC10</sub> (V)			V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)			V <sub>CM(DC)</sub> (V)			V <sub>DIF(AC)</sub> (V)	
I/O Standard	Min	Тур	Max	Min	Мах	Min	Тур	Max	Min	Тур	Max	Mi n	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.85		0.95	0.85	_	0.95	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.71		0.79	0.71	_	0.79	0.4	_
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V <sub>CCIO</sub>	0.48 x V <sub>CCIO</sub>		0.52 x V <sub>CCIO</sub>	0.48 x V <sub>CCIO</sub>		0.52 x V <sub>CCIO</sub>	0.3	0.48 x V <sub>CCIO</sub>

Note to Table 1-19:

Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices (1) (Part 1 of 2)—Preliminary

I/O Standard		V <sub>CCIO</sub> (V)	)	V <sub>ID</sub> (	V <sub>ID</sub> (mV) V <sub>IcM</sub> (V) (2)				V <sub>OD</sub> (mV) <sup>(3)</sup>			V <sub>0S</sub> (V) <sup>(3)</sup>		
i/O Stanuaru	Min Typ Max		Min	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max	
LVDEOL						0.05	$D_{MAX} \leq 500 \; Mbps$	1.80						
LVPECL (Row I/Os)	2.375	2.5	2.625	100	_	0.55	$\begin{array}{l} 500 \; \text{Mbps} \leq  D_{\text{MAX}} \\ \leq 700 \; \text{Mbps} \end{array}$	1.80	_	_	_	_	_	_
						1.05	D <sub>MAX</sub> > 700 Mbps	1.55						
IV/DEQL						0.05	$D_{MAX} \leq 500 \text{ Mbps}$	1.80						
LVPECL (Column I/Os) (6)	2.375	2.5	2.625	100	_	0.55	$\begin{array}{l} 500 \; \text{Mbps} \leq D_{\text{MAX}} \\ \leq 700 \; \text{Mbps} \end{array}$	1.80	_	_	_	_	_	_
1,00)						1.05	D <sub>MAX</sub> > 700 Mbps	1.55						
						0.05	$D_{MAX} \le 500 \text{ Mbps}$	1.80						
LVDS (Row I/Os)	2.375	2.5	2.625	100	_	0.55	$\begin{array}{l} 500 \; Mbps \leq D_{MAX} \\ \leq \; 700 \; Mbps \end{array}$	1.80	247	_	600	1.125	1.25	1.375
						1.05	$D_{MAX} > 700 \text{ Mbps}$	1.55						

<sup>(1)</sup> Differential SSTL requires a  $V_{\text{REF}}$  input.

<sup>(1)</sup> Differential HSTL requires a  $V_{\text{REF}}$  input.

Table 1-20.	Differential I/O St	andard Specifications	for Cyclone IV Devices	<i>(1)</i> (F	Part 2 of 2)—Preliminary
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I/O Ctondord		V <sub>CCIO</sub> (V)		V <sub>ID</sub> (mV)		V <sub>IcM</sub> (V) <sup>(2)</sup>				V <sub>OD</sub> (mV) <sup>(3)</sup>			V <sub>0S</sub> (V) <sup>(3)</sup>		
I/O Standard	Min	Тур	Max	Min	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max	
LVDC						0.05	$D_{MAX} \leq 500 \; Mbps$	1.80							
LVDS (Column I/Os)	2.375	2.5	2.625	100	_	0.55	$\begin{array}{l} 500 \; Mbps \leq D_{MAX} \\ \leq \; 700 \; Mbps \end{array}$	1.80	247	_	600	1.125	1.25	1.375	
1,00)						1.05	D <sub>MAX</sub> > 700 Mbps	1.55							
BLVDS (Row I/Os) (4)	2.375	2.5	2.625	100		_	_	_	_	_	_	_	_	_	
BLVDS (Column I/Os) (4)	2.375	2.5	2.625	100	_	—	_	_	_	_	_	_	—	_	
mini-LVDS (Row I/Os)	2.375	2.5	2.625	_	_	_	_	_	300	_	600	1.0	1.2	1.4	
mini-LVDS (Column I/Os) (5)	2.375	2.5	2.625	_	_	_	_	_	300	_	600	1.0	1.2	1.4	
RSDS® (Row I/Os) (5)	2.375	2.5	2.625	_		_	_	_	100	200	600	0.5	1.2	1.5	
RSDS (Column I/Os) (5)	2.375	2.5	2.625	_	_	—	_	_	100	200	600	0.5	1.2	1.5	
PPDS (Row I/Os) (5)	2.375	2.5	2.625	_	_	_	_	_	100	200	600	0.5	1.2	1.4	
PPDS (Column I/Os) (5)	2.375	2.5	2.625	_		_	_	_	100	200	600	0.5	1.2	1.4	

#### Notes to Table 1-20:

- (1) For an explanation of terms used in Table 1–20, refer to "Glossary" on page 1–38.
- (2)  $V_{IN}$  range:  $0 \text{ V} \leq V_{IN} \leq 1.85 \text{ V}.$
- (3)  $R_L$  range:  $90 \le R_L \le 110 \Omega$ .
- (4) There are no fixed  $V_{IN}$ ,  $V_{OD}$ , and  $V_{OS}$  specifications for BLVDS. They depend on the system topology.
- (5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.
- (6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

# **Power Consumption**

Use the following methods to estimate power for a design:

- the Excel-based EPE
- the Quartus<sup>®</sup> II PowerPlay power analyzer feature

The interactive Excel-based EPE is used prior to designing the device to get a magnitude estimate of the device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay power analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.



For more information about power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

# **Switching Characteristics**

This section provides performance characteristics of Cyclone IV core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The upper-right hand corner of these tables show the designation as "Preliminary".
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

# **Transceiver Performance Specifications**

Table 1–21 lists the Cyclone IV GX transceiver specifications.

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)—Preliminary

Symbol/	O a walking a		C6			C7, I7			II.a.!A		
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Reference Clock											
Supported I/O Standards		1.2 V F	PCML, 1.5	V PCML, 3	.3 V PCN	IL, Differe	ntial LVPE	CL, LVD	S, HCSL		
Input frequency from REFCLK input pins	_	50	_	156.25	50	_	156.25	50	_	156.25	MHz
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	_	33	30	_	33	30	_	33	kHz
Spread-spectrum downspread	PIPE mode	_	0 to -0.5%	_	_	0 to -0.5%	_	_	0 to -0.5%	_	_
V <sub>ICM</sub> (AC coupled)			1100 ± 5	5%		1100 ± 5%	<b>%</b>		1100 ± 5	%	mV
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	250	_	550	mV
Transmitter REFCLK Phase Noise <sup>(1)</sup>	Frequency offset	_	_	-123	_	_	-123	_	_	-123	dBc/Hz
Transmitter REFCLK Total Jitter <sup>(1)</sup>	= 1 MHz – 8 MHZ	_	_	42.3	_	_	42.3	_	_	42.3	ps
R <sub>ref</sub>	_	_	2000 ± 1%	_	_	2000 ± 1%	_	_	2000 ± 1%	_	Ω
Transceiver Clock											
cal_blk_clk clock frequency	_	10	_	125	10	_	125	10	_	125	MHz
fixedclk Clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	_	125	_	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 (2)	_	50	2.5/ 37.5 (2)	_	50	2.5/ 37.5 (2)	_	50	MHz
Delta time between reconfig_clk	_	_	_	2	_	_	2	_	_	2	ms
Transceiver block minimum power-down pulse width	_		1	-	_	1	_		1	_	μѕ
Receiver						_					
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)—Preliminary

Symbol/	0 1111		C6			C7, I7			C8		llmit
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Data rate (F324 and smaller package)	_	600	_	2500	600	_	2500	600	_	2500	Mbps
Data rate (F484 and larger package)	_	600	_	3125	600	_	3125	600	_	2500	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(3)</sup>	_	_	_	1.6	_	_	1.6	_	_	1.6	V
Operational V <sub>MAX</sub> for a receiver pin	_	_	_	1.5	_	_	1.5	_	_	1.5	V
Absolute V <sub>MIN</sub> for a receiver pin	_	-0.4	_	_	-0.4	_	_	-0.4	_	_	V
Peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p)	V <sub>ICM</sub> = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps	0.1	_	2.7	0.1	_	2.7	0.1	_	2.7	V
V <sub>ICM</sub>	V <sub>ICM</sub> = 0.82 V setting	_	820 ± 10%	_	_	820 ± 10%	_	_	820 ± 10%	_	mV
Differential on-chip	100– $\Omega$ setting		100	_	_	100	_	_	100	_	Ω
termination resistors	150– $\Omega$ setting	_	150	_	_	150		_	150	_	Ω
Differential and common mode return loss	PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI					Compliant	t				_
Programmable ppm detector <sup>(4)</sup>	_				± 62.5	, 100, 125 250, 300	5, 200,				ppm
Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)	_		_	±300 (5), ±350 (6), (7)	_	_	±300 (5), ±350 (6), (7)	_	_	±300 (5), ±350 (6), (7)	ppm
CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) (8)	_	_	_	350 to -5350 (7), (9)	_	_	350 to -5350 (7), (9)	_	_	350 to -5350 (7), (9)	ppm
Run length	_		80	_	_	80	_	_	80	_	UI
	No Equalization		_	1.5	_	_	1.5	_	_	1.5	dB
Programmable	Medium Low	_	_	4.5	_	_	4.5	_	_	4.5	dB
equalization	Medium High	_		5.5			5.5	_		5.5	dB
	High		_	7	_	_	7	_	_	7	dB
Signal detect/loss threshold	PIPE mode	65		175	65	_	175	65		175	mV
t <sub>LTR</sub> (10)	_			75		_	75	_	_	75	μs
t <sub>LTR-LTD_Manual</sub> (11)	_	15		_	15			15		_	μs
t <sub>LTD</sub> (12)	_	0	100	4000	0	100	4000	0	100	4000	ns

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 3 of 4)—Preliminary

Symbol/	O a waliki a wa		C6			C7, I7				Unit	
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t <sub>LTD_Manual</sub> (13)	_	_	_	4000	_	_	4000	_	_	4000	ns
t <sub>LTD_Auto</sub> (14)	_	_	_	4000	_	_	4000	_	_	4000	ns
Receiver buffer and CDR offset cancellation time (per channel)	_	_	_	17000	_	_	17000	_	_	17000	recon fig_c lk cycles
	DC Gain Setting = 0	_	0	_	_	0	_	_	0	_	dB
Programmable DC gain	DC Gain Setting = 1	_	3	_	_	3	_	_	3	_	dB
	DC Gain Setting = 2	_	6	_	_	6	_	_	6	_	dB
Transmitter						•	•			•	•
Supported I/O Standards	1.5 V PCML										
Data rate (F324 and smaller package)	_	600	_	2500	600	_	2500	600	_	2500	Mbps
Data rate (F484 and larger package)	_	600	_	3125	600	_	3125	600	_	2500	Mbps
V <sub>OCM</sub>	0.65 V setting	_	650	_	_	650	_	_	650	_	mV
Differential on-chip	100–Ω setting	_	100	_	_	100		_	100	_	Ω
termination resistors	150– $\Omega$ setting	_	150	_	_	150	_	_	150	_	Ω
Differential and common mode return loss	PIPE, CPRI LV, Serial Rapid I/O SR, SDI, XAUI, SATA					Compliant	İ				_
Rise time	_	50	_	200	50	_	200	50	_	200	ps
Fall time	_	50	_	200	50	_	200	50	_	200	ps
Intra-differential pair skew	_	_	_	15	_	_	15	_	_	15	ps
Intra-transceiver block skew	_	_	_	120	_	_	120	_	_	120	ps

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)—Preliminary

Symbol/	Conditions		C6		C7, I7			C8			Unit
Description	Collultions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
PLD-Transceiver Inte	rface										
Interface speed (F324 and smaller package)	_	25	_	125	25	_	125	25	_	125	MHz
Interface speed (F484 and larger package)	_	25	_	156.25	25	_	156.25	25	_	156.25	MHz
Digital reset pulse width	_		Minimum is 2 parallel clock cycles								

#### Notes to Table 1-21:

- (1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.
- (2) The minimum reconfig\_clk frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum reconfig\_clk frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The rate matcher supports only up to ±300 parts per million (ppm).
- (5) Supported for the N148, F169, and F324 device packages only.
- (6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.
- (7) To support CDR ppm tolerance greater than ±300 ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.
- (8) Asynchronous spread-spectrum clocking is not supported.
- (9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is ±200 ppm.
- (10) Time taken until pll locked goes high after pll powerdown deasserts.
- (11) Time that the CDR must be kept in lock-to-reference mode after rx analogreset deasserts and before rx locktodata is asserted in manual mode.
- (12) Time taken to recover valid data after the rx\_locktodata signal is asserted in manual mode (Figure 1–2), or after rx\_freqlocked signal goes high in automatic mode (Figure 1–3).
- (13) Time taken to recover valid data after the  $rx\_locktodata$  signal is asserted in manual mode.
- (14) Time taken to recover valid data after the  $rx_freqlocked$  signal goes high in automatic mode.

Figure 1–2 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.

Figure 1–2. Lock Time Parameters for Manual Mode

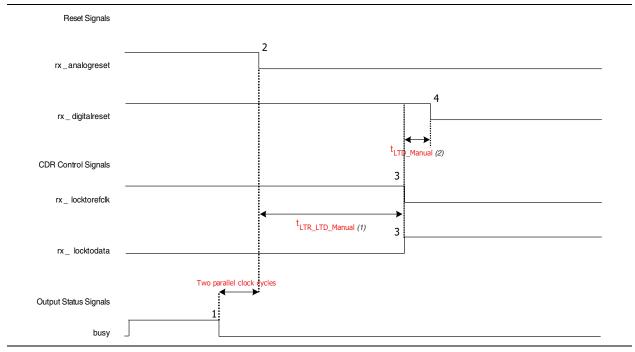


Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode

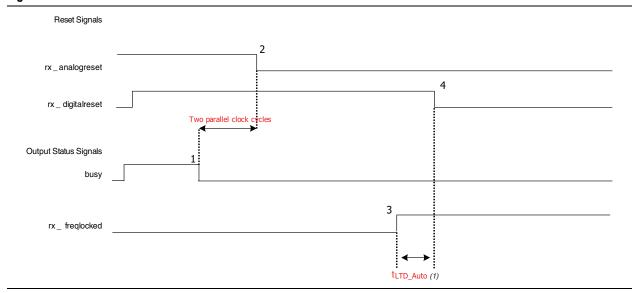


Figure 1–4 shows the differential receiver input waveform.

Figure 1-4. Receiver Input Waveform

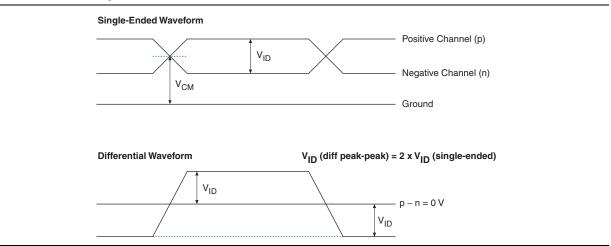


Figure 1–5 shows the transmitter output waveform.

Figure 1-5. Transmitter Output Waveform—Preliminary

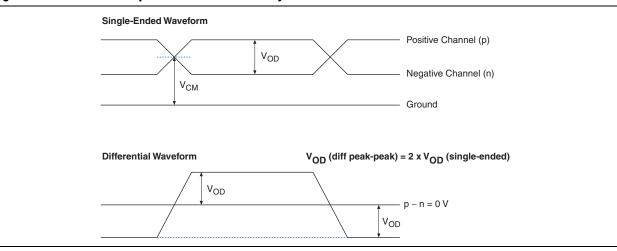


Table 1–22 lists the typical  $V_{OD}$  for Tx term that equals 100  $\Omega$ ..

Table 1–22. Typical  $V_{0D}$  Setting, Tx Term = 100  $\Omega$  —Preliminary

Symbol		V <sub>OD</sub> Setting (mV)										
Symbol	1	2	3	4 (1)	5	6						
V <sub>OD</sub> Typical (mV)	400	600	800	900	1000	1200						

#### Note to Table 1-22:

(1) This setting is required for compliance with the PCIe protocol.

Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices (1), (2) —Preliminary

Symbol/	Conditions		C6			C7, I7	7		Unit		
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
PCIe Transmit Jitter Gene	ration <sup>(3)</sup>										
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	_		0.25	_	_	0.25	_	_	0.25	UI
PCIe Receiver Jitter Toler	ance <sup>(3)</sup>										
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6	6		> 0.6	i		> 0.6	6	UI
GIGE Transmit Jitter Gene	ration <sup>(4)</sup>										
Deterministic jitter	Pattern = CRPAT		_	0.14			0.14			0.14	UI
(peak-to-peak)	Tattom - On 70			0.11			0.11			0.11	01
Total jitter (peak-to-peak)	Pattern = CRPAT	_	_	0.279	_	_	0.279	_	_	0.279	UI
GIGE Receiver Jitter Toler	ance <sup>(4)</sup>										
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.4		> 0.4				> 0.4	ļ	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66		> 0.66			> 0.66			UI	

#### Notes to Table 1-23:

- (1) Dedicated refclk pins were used to drive the input reference clocks.
- (2) The jitter numbers specified are valid for the stated conditions only.
- (3) The jitter numbers for PIPE are compliant to the PCle Base Specification 2.0.
- (4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

## **Core Performance Specifications**

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

## **Clock Tree Specifications**

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)—Preliminary

Dovice		Performance												
Device	C6	<b>C</b> 7	C8	C8L (1)	C9L (1)	17	I8L <sup>(1)</sup>	A7	Unit					
EP4CE6	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE10	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE15	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE22	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE30	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE40	500	437.5	402	362	265	437.5	362	402	MHz					

Davisa		Performance											
Device	C6	<b>C</b> 7	C8	C8L (1)	C9L (1)	17	I8L (1)	A7	Unit				
EP4CE55	500	437.5	402	362	265	437.5	362	_	MHz				
EP4CE75	500	437.5	402	362	265	437.5	362	_	MHz				
EP4CE115	_	437.5	402	362	265	437.5	362	_	MHz				
EP4CGX15	500	437.5	402	_	_	437.5	_	_	MHz				
EP4CGX22	500	437.5	402	_	_	437.5	_	_	MHz				
EP4CGX30	500	437.5	402	_	_	437.5	_	_	MHz				
EP4CGX50	500	437.5	402	_	_	437.5	_	_	MHz				
EP4CGX75	500	437.5	402	_	_	437.5	_	_	MHz				
EP4CGX110	500	437.5	402	_	_	437.5	_	_	MHz				
EP4CGX150	500	437.5	402	_	_	437.5		_	MHz				

Table 1-24. Clock Tree Performance for Cyclone IV Devices (Part 2 of 2)—Preliminary

#### Note to Table 1-24:

## **PLL Specifications**

Table 1–25 lists the PLL specifications for Cyclone IV devices when operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (-40°C to 100°C), the extended industrial junction temperature range (-40°C to 125°C), and the automotive junction temperature range (-40°C to 125°C). For more information about the PLL block, refer to "Glossary" on page 1–38.

Table 1–25. PLL Specifications for Cyclone IV Devices (1), (2) (Part 1 of 2)—Preliminary

Symbol	Parameter	Min	Тур	Max	Unit
	Input clock frequency (-6, -7, -8 speed grades)	5	_	472.5	MHz
f <sub>IN</sub> (3)	Input clock frequency (-8L speed grade)	5	_	362	MHz
	Input clock frequency (–9L speed grade)	5	_	265	MHz
f <sub>INPFD</sub>	PFD input frequency	5	_	325	MHz
f <sub>VCO</sub> (4)	PLL internal VCO operating range	600	_	1300	MHz
f <sub>INDUTY</sub>	Input clock duty cycle	40	_	60	%
t <sub>INJITTER_CCJ</sub> (5)	Input clock cycle-to-cycle jitter F <sub>REF</sub> ≥ 100 MHz	_	_	0.15	UI
	F <sub>REF</sub> < 100 MHz	_	_	±750	ps
f <sub>OUT_EXT</sub> (external clock output) <sup>(3)</sup>	PLL output frequency	_	_	472.5	MHz
	PLL output frequency (-6 speed grade)	_	_	472.5	MHz
	PLL output frequency (-7 speed grade)	_	_	450	MHz
f <sub>OUT</sub> (to global clock)	PLL output frequency (-8 speed grade)	_	_	402.5	MHz
	PLL output frequency (-8L speed grade)	_	_	362	MHz
	PLL output frequency (-9L speed grade)	_	_	265	MHz
t <sub>OUTDUTY</sub>	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t <sub>LOCK</sub>	Time required to lock from end of device configuration	_	_	1	ms

<sup>(1)</sup> Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades.

Table 1–25. PLL Specifications for Cyclone IV Devices (1), (2) (Part 2 of 2)—Preliminary

Symbol	Parameter	Min	Тур	Max	Unit
t <sub>DLOCK</sub>	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted)	_	_	1	ms
toutjitter_period_dedclk (6)	Dedicated clock output period jitter $F_{OUT} \ge 100 \text{ MHz}$	_	_	300	ps
	F <sub>OUT</sub> < 100 MHz	_	_	30	mUI
toutjitter_ccj_dedclk (6)	Dedicated clock output cycle-to-cycle jitter F <sub>OUT</sub> ≥ 100 MHz	_	_	300	ps
	F <sub>OUT</sub> < 100 MHz	_	_	30	mUI
t <sub>OUTJITTER_PERIOD_IO</sub> (6)	Regular I/O period jitter $F_{OUT} \ge 100 \text{ MHz}$	_	_	650	ps
	F <sub>OUT</sub> < 100 MHz	_	_	75	mUI
toutjitter_ccj_io (6)	Regular I/O cycle-to-cycle jitter $F_{OUT} \ge 100 \text{ MHz}$	_	_	650	ps
	F <sub>OUT</sub> < 100 MHz	_	_	75	mUI
t <sub>PLL_PSERR</sub>	Accuracy of PLL phase shift	_	_	±50	ps
t <sub>ARESET</sub>	Minimum pulse width on areset signal.	10	_	_	ns
t <sub>CONFIGPLL</sub>	Time required to reconfigure scan chains for PLLs	_	3.5 (7)		SCANCLK cycles
f <sub>SCANCLK</sub>	scanclk frequency	_	_	100	MHz
t <sub>CASC_</sub> OUTJITTER_PERIOD_DEDCLK	Period jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} \ge 100 \text{ MHz}$ )	_	_	425	ps
(8), (9)	Period jitter for dedicated clock output in cascaded PLLs (F <sub>OUT</sub> < 100 MHz)	_	_	42.5	mUI

#### Notes to Table 1-25:

- (1) This table is applicable for general purpose PLLs and multipurpose PLLs.
- (2) You must connect  $V_{CCD\ PLL}$  to  $V_{CCINT}$  through the decoupling capacitor and ferrite bead.
- (3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (4) The  $V_{CO}$  frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the  $V_{CO}$  post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.
- (5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.
- (6) Peak-to-peak jitter with a probability level of 10<sup>-12</sup> (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.
- (7) With 100-MHz scanclk frequency.
- $\begin{tabular}{ll} (8) & The cascaded PLLs specification is applicable only with the following conditions: \end{tabular}$ 
  - $\qquad \text{Upstream PLL--0.59 MHz} \leq \text{Upstream PLL bandwidth} < 1 \text{ MHz}$
  - Downstream PLL—Downstream PLL bandwidth > 2 MHz
- (9) PLL cascading is not supported for transceiver applications.

## **Embedded Multiplier Specifications**

Table 1–26 lists the embedded multiplier specifications for Cyclone IV devices.

Table 1–26. Embedded Multiplier Specifications for Cyclone IV Devices —Preliminary

Mode	Resources Used		Performance							
Mode	Number of Multipliers	C6	C7, I7, A7	C8	C8L, I8L	C9L	Unit			
9 × 9-bit multiplier	1	340	300	260	240	175	MHz			
18 × 18-bit multiplier	1	287	250	200	185	135	MHz			

### **Memory Block Specifications**

Table 1–27 lists the M9K memory block specifications for Cyclone IV devices.

Table 1–27. Memory Block Performance Specifications for Cyclone IV Devices —Preliminary

		Resou	rces Used		Per	formar	ice		
Memory	Mode	LEs	M9K Memory	C6	C7, I7, A7	C8	C8L, I8L	C9L	Unit
	FIFO 256 × 36	47	1	315	274	238	200	157	MHz
M9K Block	Single-port 256 × 36	0	1	315	274	238	200	157	MHz
INISK DIOCK	Simple dual-port 256 × 36 CLK	0	1	315	274	238	200	157	MHz
	True dual port 512 × 18 single CLK	0	1	315	274	238	200	157	MHz

### **Configuration and JTAG Specifications**

Table 1–28 lists the configuration mode specifications for Cyclone IV devices.

Table 1–28. Passive Configuration Mode Specifications for Cyclone IV Devices (1)

Programming Mode	V <sub>CCINT</sub> Voltage Level (V)	DCLK f <sub>max</sub>	Unit
Passive Serial (PS)	1.0 <sup>(3)</sup>	66	MHz
rassive serial (rs)	1.2	133	MHz
Fast Passive Parallel (FPP) (2)	1.0 <sup>(3)</sup>	66	MHz
Table rassive ratallet (FFF) 1-7	1.2 <sup>(4)</sup>	100	MHz

#### Notes to Table 1-28:

- (1) For more information about PS and FPP configuration timing parameters, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.
- (2) FPP configuration mode supports all Cyclone IV E devices (except for E144 package devices) and EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 only.
- (3)  $V_{CCINT} = 1.0 \text{ V}$  is only supported for Cyclone IV E 1.0 V core voltage devices.
- (4) Cyclone IV E devices support 1.2 V V<sub>CCINT</sub>. Cyclone IV E 1.2 V core voltage devices support 133 MHz DCLK f<sub>MAX</sub> for EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, and EP4CE40 only.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

Table 1-29. Active Configuration Mode Specifications for Cyclone IV Devices—Preliminary

Programming Mode	DCLK Range	Unit
Active Parallel (AP) (1)	20 to 40	MHz
Active Serial (AS)	20 to 40	MHz

#### Note to Table 1-29:

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

Table 1–30. JTAG Timing Parameters for Cyclone IV Devices (1) —Preliminary

Symbol	Parameter	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period	40	_	ns
t <sub>JCH</sub>	TCK clock high time	19	_	ns
t <sub>JCL</sub>	TCK clock low time	19	_	ns
t <sub>JPSU_TDI</sub>	JTAG port setup time for TDI	1	_	ns
t <sub>JPSU_TMS</sub>	JTAG port setup time for TMS	3	_	ns
$t_{JPH}$	JTAG port hold time	10	_	ns
t <sub>JPCO</sub>	JTAG port clock to output (2), (3)	_	15	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output (2), (3)	_	15	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance (2), (3)	_	15	ns
t <sub>JSSU</sub>	Capture register setup time	5	_	ns
t <sub>JSH</sub>	Capture register hold time	10	_	ns
t <sub>JSCO</sub>	Update register clock to output	_	25	ns
t <sub>JSZX</sub>	Update register high impedance to valid output	_	25	ns
t <sub>JSXZ</sub>	Update register valid output to high impedance	_	25	ns

#### Notes to Table 1-30:

- (1) For more information about JTAG waveforms, refer to "JTAG Waveform" in "Glossary" on page 1-38.
- (2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.
- (3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

## **Periphery Performance**

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.



For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.



Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### **High-Speed I/O Specifications**

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to "Glossary" on page 1–38.

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 1 of 2)—Preliminary

Ob.al	Madaa		C6			C7, I	7		C8, A	7		C8L, I	BL		C9L		11!4
Symbol	Modes	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
	×10	10	_	180	10	_	155.5	10	_	155.5	10	_	155.5	10	_	132.5	MHz
	×8	10		180	10	_	155.5	10	_	155.5	10		155.5	10	_	132.5	MHz
f <sub>HSCLK</sub> (input clock	×7	10		180	10	_	155.5	10		155.5	10		155.5	10	_	132.5	MHz
frequency)	×4	10		180	10	_	155.5	10		155.5	10	-	155.5	10	-	132.5	MHz
,	×2	10	_	180	10	_	155.5	10		155.5	10	_	155.5	10	_	132.5	MHz
	×1	10	_	360	10	_	311	10		311	10	-	311	10	-	265	MHz
	×10	100	_	360	100	_	311	100	l	311	100	_	311	100	_	265	Mbps
	×8	80	_	360	80	_	311	80	l	311	80		311	80		265	Mbps
Device operation in	×7	70		360	70	_	311	70		311	70	1	311	70	1	265	Mbps
Mbps	×4	40	_	360	40	_	311	40		311	40	_	311	40	_	265	Mbps
·	×2	20	_	360	20	_	311	20	_	311	20	_	311	20	_	265	Mbps
	×1	10		360	10		311	10		311	10		311	10		265	Mbps
t <sub>DUTY</sub>	_	45	_	55	45	_	55	45		55	45	_	55	45	_	55	%
Transmitter channel-to- channel skew (TCCS)	_	_	_	200	_	_	200			200	_		200	_		200	ps
Output jitter (peak to peak)	_	_	_	500	_	_	500	_	_	550	_	_	600	_	_	700	ps
t <sub>RISE</sub>	20 – 80%, C <sub>LOAD</sub> = 5 pF	_	500	_	_	500	_	_	500	_	_	500	_	_	500	_	ps
t <sub>FALL</sub>	20 – 80%, C <sub>LOAD</sub> = 5 pF	_	500	_	_	500	_	_	500	_	_	500	_	_	500	_	ps

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 2 of 2)—Preliminary

Symbol	Modes		C6			C7, I	7		C8, A	7		C8L, I	BL		C9L		Unit
Syllibul	MOUGS	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIII
t <sub>LOCK</sub> (3)	_	_	_	1	_	_	1	_	_	1	_	_	1	_	_	1	ms

#### Notes to Table 1-31:

- (1) Applicable for true RSDS and emulated RSDS\_E\_3R transmitter.
- (2) Cyclone IV E devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks.

  Cyclone IV GX devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (3)  $t_{LOCK}$  is the time required for the PLL to lock from the end-of-device configuration.
- (4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–32. Emulated RSDS\_E\_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 1 of 2) —Preliminary

Combal	Madaa		C6			C7, 17	ı		C8, A7	7	(	C8L, 18	BL		C9L		Unit
Symbol	Modes	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
	×10	10	_	85	10	_	85	10	_	85	10	_	85	10	_	72.5	MHz
	×8	10	_	85	10	_	85	10	_	85	10	_	85	10	_	72.5	MHz
f <sub>HSCLK</sub> (input clock	×7	10	_	85	10	_	85	10		85	10		85	10	_	72.5	MHz
frequency)	×4	10	_	85	10	_	85	10		85	10		85	10	_	72.5	MHz
. 37	×2	10	_	85	10	_	85	10	_	85	10		85	10	_	72.5	MHz
	×1	10	_	170	10	_	170	10	_	170	10		170	10	_	145	MHz
	×10	100	_	170	100	_	170	100	_	170	100	_	170	100	_	145	Mbps
	×8	80	_	170	80	_	170	80	_	170	80		170	80	_	145	Mbps
Device operation in	×7	70	_	170	70	_	170	70	_	170	70		170	70	_	145	Mbps
Mbps	×4	40		170	40	_	170	40		170	40	_	170	40		145	Mbps
	×2	20	_	170	20	_	170	20	_	170	20	_	170	20	_	145	Mbps
	×1	10	_	170	10	_	170	10	_	170	10	_	170	10	_	145	Mbps
t <sub>DUTY</sub>	_	45		55	45	_	55	45		55	45	_	55	45		55	%
TCCS	_	_	_	200	_	_	200	_	_	200	_	_	200	_	_	200	ps
Output jitter (peak to peak)	_	_	_	500	_	_	500	_	_	550	_	_	600	_	_	700	ps
t <sub>RISE</sub>	$20 - 80\%$ , $C_{LOAD} = 5 pF$	_	500		_	500		_	500	_	_	500	_	_	500	_	ps
t <sub>FALL</sub>	$20 - 80\%$ , $C_{LOAD} = 5 pF$	_	500		_	500		_	500	_	_	500	_	_	500	_	ps

Table 1–32. Emulated RSDS\_E\_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2) —Preliminary

Symbol	Modes		C6			C7, 17	'		C8, A7	7	(	C8L, 18	SL.		C9L		Unit
	Mones	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Ullit
t <sub>LOCK</sub> (2)	_	_		1	_		1	_		1	_	_	1	_		1	ms

#### Notes to Table 1-32:

- (1) Emulated RSDS\_E\_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.
- (2)  $t_{LOCK}$  is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 1 of 2)—Preliminary

Combal	Madaa		C6			C7, I	7		C8, A	7		C8L, I	8L		C9L		II.a.i.t
Symbol	Modes	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
	×10	10	_	200	10		155.5	10	_	155.5	10	_	155.5	10	_	132.5	MHz
	×8	10	_	200	10		155.5	10	_	155.5	10	_	155.5	10	_	132.5	MHz
f <sub>HSCLK</sub> (input clock	×7	10	_	200	10	_	155.5	10	_	155.5	10	_	155.5	10	_	132.5	MHz
frequency)	×4	10	_	200	10		155.5	10		155.5	10	_	155.5	10	_	132.5	MHz
. ,,	×2	10	_	200	10	_	155.5	10	_	155.5	10	_	155.5	10	_	132.5	MHz
	×1	10	_	400	10	_	311	10	_	311	10	_	311	10	_	265	MHz
	×10	100	_	400	100		311	100		311	100	_	311	100	_	265	Mbps
	×8	80	_	400	80		311	80	_	311	80	_	311	80	_	265	Mbps
Device operation in	×7	70	_	400	70		311	70	_	311	70	_	311	70	_	265	Mbps
Mbps	×4	40	_	400	40		311	40		311	40	_	311	40	_	265	Mbps
	×2	20	_	400	20	_	311	20	_	311	20	_	311	20	_	265	Mbps
	×1	10	_	400	10	_	311	10	_	311	10	_	311	10	_	265	Mbps
t <sub>DUTY</sub>	_	45	_	55	45		55	45	_	55	45		55	45	_	55	%
TCCS	_		1	200	_	_	200		_	200		_	200	_		200	ps
Output jitter (peak to peak)	_	-		500	_	_	500		_	550	_	_	600	_		700	ps
t <sub>RISE</sub>	20 – 80%, C <sub>LOAD</sub> = 5 pF	_	500	_	_	500		_	500	_	_	500	_	_	500	_	ps
t <sub>FALL</sub>	20 – 80%, C <sub>LOAD</sub> = 5 pF	_	500	_	_	500	_	_	500	_	_	500	_	_	500	_	ps

Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 2 of 2)—Preliminary

	Cumbal	Modes		C6			C7, I7	7		C8, A	7		C8L, I	8L		C9L		Unit
Symbol	MOUGS	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Ullit	
	t <sub>LOCK</sub> (3)	_	_		1		_	1	_	_	1		_	1	_	_	1	ms

#### Notes to Table 1-33:

- (1) Applicable for true and emulated mini-LVDS transmitter.
- (2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.

  Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (3)  $t_{LOCK}$  is the time required for the PLL to lock from the end-of-device configuration.
- (4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (3) —Preliminary

Obal	Madaa	C	6	C7	, I7	C8,	, A7	C8L	, I8L	C	9L	11!4
Symbol	Modes	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
	×10	10	420	10	370	10	320	10	320	10	250	MHz
	×8	10	420	10	370	10	320	10	320	10	250	MHz
f <sub>HSCLK</sub> (input	×7	10	420	10	370	10	320	10	320	10	250	MHz
clock frequency)	×4	10	420	10	370	10	320	10	320	10	250	MHz
,,	×2	10	420	10	370	10	320	10	320	10	250	MHz
	×1	10	420	10	402.5	10	402.5	10	362	10	265	MHz
	×10	100	840	100	740	100	640	100	640	100	500	Mbps
	×8	80	840	80	740	80	640	80	640	80	500	Mbps
HCIODD	×7	70	840	70	740	70	640	70	640	70	500	Mbps
HSIODR	×4	40	840	40	740	40	640	40	640	40	500	Mbps
	×2	20	840	20	740	20	640	20	640	20	500	Mbps
	×1	10	420	10	402.5	10	402.5	10	362	10	265	Mbps
t <sub>DUTY</sub>	_	45	55	45	55	45	55	45	55	45	55	%
TCCS	_	_	200	_	200		200		200	_	200	ps
Output jitter (peak to peak)	_	_	500	_	500	_	550	_	600	_	700	ps
t <sub>LOCK</sub> (2)		_	1	_	1	_	1	_	1	_	1	ms

#### Notes to Table 1-34:

- (1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.
- (2)  $t_{LOCK}$  is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (3) —Preliminary

Cumbal	Madaa	C	6	<b>C</b> 7,	, I7	C8,	A7	C8L	, I8L	C	9L	II.u.i.t
Symbol	Modes	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
	×10	10	320	10	320	10	275	10	275	10	250	MHz
	×8	10	320	10	320	10	275	10	275	10	250	MHz
f <sub>HSCLK</sub> (input	×7	10	320	10	320	10	275	10	275	10	250	MHz
clock frequency)	×4	10	320	10	320	10	275	10	275	10	250	MHz
, ,,	×2	10	320	10	320	10	275	10	275	10	250	MHz
	×1	10	402.5	10	402.5	10	402.5	10	362	10	265	MHz
	×10	100	640	100	640	100	550	100	550	100	500	Mbps
	×8	80	640	80	640	80	550	80	550	80	500	Mbps
HSIODR	×7	70	640	70	640	70	550	70	550	70	500	Mbps
поиори	×4	40	640	40	640	40	550	40	550	40	500	Mbps
	×2	20	640	20	640	20	550	20	550	20	500	Mbps
	×1	10	402.5	10	402.5	10	402.5	10	362	10	265	Mbps
t <sub>DUTY</sub>	_	45	55	45	55	45	55	45	55	45	55	%
TCCS	_	_	200	_	200	_	200	_	200	_	200	ps
Output jitter (peak to peak)	_	_	500	_	500	_	550	_	600	_	700	ps
t <sub>LOCK</sub> (2)	_		1		1		1		1		1	ms

#### Notes to Table 1-35:

- Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.
   Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2)  $t_{LOCK}$  is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices (1), (3) (Part 1 of 2)—Preliminary

Combal	Madaa	C	6	<b>C</b> 7,	, <b>17</b>	C8,	<b>A</b> 7	C8L	, I8L	C	)L	Unit
Symbol	Modes	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	×10	10	437.5	10	370	10	320	10	320	10	250	MHz
	×8	10	437.5	10	370	10	320	10	320	10	250	MHz
f <sub>HSCLK</sub> (input	×7	10	437.5	10	370	10	320	10	320	10	250	MHz
clock frequency)	×4	10	437.5	10	370	10	320	10	320	10	250	MHz
, ,	×2	10	437.5	10	370	10	320	10	320	10	250	MHz
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	MHz
	×10	100	875	100	740	100	640	100	640	100	500	Mbps
	×8	80	875	80	740	80	640	80	640	80	500	Mbps
HSIODR	×7	70	875	70	740	70	640	70	640	70	500	Mbps
нэшик	×4	40	875	40	740	40	640	40	640	40	500	Mbps
	×2	20	875	20	740	20	640	20	640	20	500	Mbps
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	Mbps

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C	Unit	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
SW	_	_	400	_	400	_	400	_	550	_	640	ps
Input jitter tolerance	_	_	500	_	500	_	550	_	600	_	700	ps
t <sub>LOCK</sub> (2)	_		1		1	_	1	_	1	_	1	ms

#### Notes to Table 1-36:

- (1) Cyclone IV E—LVDS receiver is supported at all I/O Banks. Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2)  $t_{LOCK}$  is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

### **External Memory Interface Specifications**

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.



For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to Section III: System Performance Specifications of the External Memory Interface Handbook.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices (1), (2) — **Preliminary** 

Parameter	Symbol	Min	Max	Unit
Clock period jitter	t <sub>JIT(per)</sub>	-125	125	ps
Cycle-to-cycle period jitter	t <sub>JIT(cc)</sub>	-200	200	ps
Duty cycle jitter	t <sub>JIT(duty)</sub>	-150	150	ps

#### Notes to Table 1-37:

- (1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2
- (2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

### **Duty Cycle Distortion Specifications**

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins (1), (2), (3)—Preliminary

Symbol	C	6	<b>C</b> 7	, I7	C8, I8	BL, A7	C	llmit	
	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Output Duty Cycle	45	55	45	55	45	55	45	55	%

#### Notes to Table 1-38:

- (1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.
- (2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

### **OCT Calibration Timing Specification**

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices  $^{(1)}$ —Preliminary

Symbol	Description	Maximum	Units
t <sub>OCTCAL</sub>	Duration of series OCT with calibration at device power-up	20	μs

#### Note to Table 1-39:

 $(1) \quad \text{OCT calibration takes place after device configuration and before entering user mode}.$ 

## IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices (1), (2) (Part 1 of 2)—Preliminary

		Number of Setting	Min Offset	Max Offset						
Parameter	Paths Affected			Fast Corner		S	Unit			
				C8L	I8L	C8L	C9L	I8L		
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.054	1.924	3.387	4.017	3.411	ns	
Input delay from pin to input register	Pad to I/O input register	8	0	2.010	1.875	3.341	4.252	3.367	ns	
Delay from output register to output pin	I/O output register to pad	2	0	0.641	0.631	1.111	1.377	1.124	ns	

Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices (1), (2) (Part 2 of 2)—Preliminary

Parameter		Number	Min Offset	Max Offset						
	Paths Affected	of Setting		Fast Corner		Slow Corner			Unit	
				C8L	I8L	C8L	C9L	I8L		
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.971	0.931	1.684	2.298	1.684	ns	

#### Notes to Table 1-40:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices (1). (2)—Preliminary

		Number of Setting	Min Offset	Max Offset						
Parameter	Paths Affected			Fast (	Corner	S	Unit			
				C8L	I8L	C8L	C9L	I8L		
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.057	1.921	3.389	4.146	3.412	ns	
Input delay from pin to input register	Pad to I/O input register	8	0	2.059	1.919	3.420	4.374	3.441	ns	
Delay from output register to output pin	I/O output register to pad	2	0	0.670	0.623	1.160	1.420	1.168	ns	
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.960	0.919	1.656	2.258	1.656	ns	

#### Notes to Table 1-41:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting  $\bf 0$  as available in the Quartus II software.

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E  $1.2~\rm V$  core voltage devices.

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices (1), (2) (Part 1 of 2)—Preliminary

Parameter		Number	Min				Max (	Offset				
	Paths Affected	of Setting		Fa	ast Corn	er		Unit				
				C6	17	A7	C6	<b>C</b> 7	C8	17	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices  $^{(1), (2)}$  (Part 2 of 2)—Preliminary

Parameter		Number Number		Max Offset								
	Paths of Affected Setti	of	of Min	Fact linthor			Slow Corner					
		Setting		C6	17	A7	C6	<b>C</b> 7	C8	17	A7	
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

#### Notes to Table 1-42:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices (1), (2)—Preliminary

		Number	Min	Max Offset									
Parameter	Paths Affected	of Setting		Fa	ast Corn	er		Unit					
				C6	17	A7	C6	<b>C</b> 7	C8	17	A7		
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns	
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns	
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns	
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns	

#### Notes to Table 1-43:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices (1), (2) (Part 1 of 2)—Preliminary

		Number		Max Offset						
Parameter	Paths Affected	of	Min Offset	Fast (	Corner	Slow Corner				Unit
		Settings		C6	17	C6	C7	C8	17	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	1.209	2.184	2.336	2.451	2.387	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.208	2.200	2.399	2.554	2.446	ns

Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices (1), (2) (Part 2 of 2)—Preliminary

		Number		Max Offset						
Parameter	Paths Affected	of	Min Offset	Fast Corner		Slow Corner				Unit
	Allocton		Settings		17	C6	<b>C</b> 7	C8	17	
Delay from output register to output pin	I/O output register to pad	2	0	0.438	0.404	0.751	0.825	0.886	0.839	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.713	0.682	1.228	1.41	1.566	1.424	ns

#### Notes to Table 1-44:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices (1), (2) —Preliminary

		Number		Max Offset						Unit
Parameter	Paths Affected	ns of		Fast Corner		Slow Corner				
				C6	17	C6	C7	C8	17	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.210	2.209	2.398	2.526	2.443	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.313	1.208	2.205	2.406	2.563	2.450	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.461	0.421	0.789	0.869	0.933	0.884	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.712	0.682	1.225	1.407	1.562	1.421	ns

#### Notes to Table 1-45:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting 0 as available in the Quartus II software

## I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.



The Excel-based I/O Timing spreadsheet is downloadable from Cyclone IV Devices Literature website.

## **Glossary**

Table 1–46 lists the glossary for this chapter.

Table 1-46. Glossary (Part 1 of 5)

Letter	Term	Definitions						
Α	_	_						
В	_	_						
С	_	_						
D	_	_						
E	_	_						
F	f <sub>HSCLK</sub>	High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.						
G	GCLK	Input pin directly to Global Clock network.						
u u	GCLK PLL	Input pin to Global Clock network through the PLL.						
Н	HSIODR	High-speed I/O block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI).						
I	Input Waveforms for the SSTL Differential I/O Standard	Vswing V <sub>IH</sub>						

Table 1-46. Glossary (Part 2 of 5)

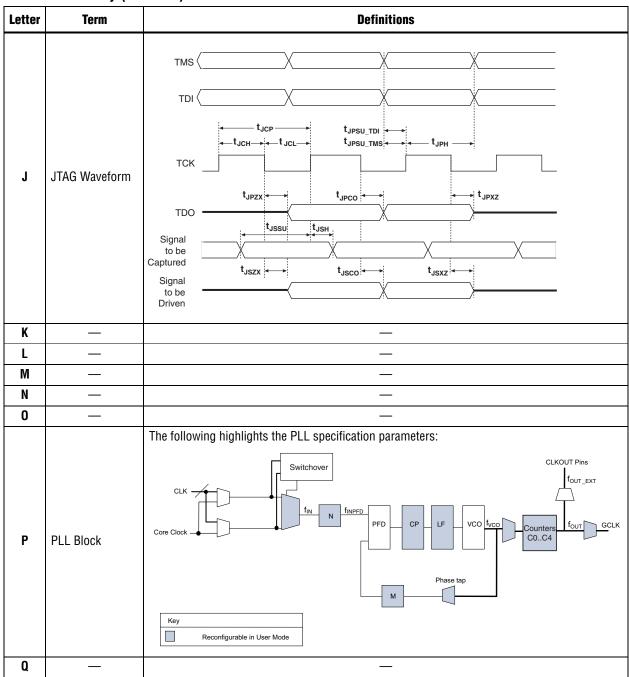


Table 1-46. Glossary (Part 3 of 5)

Letter	Term	Definitions								
	R <sub>L</sub>	Receiver differential input discrete resistor (external to Cyclone IV devices).								
		Receiver input waveform for LVDS and LVPECL differential standards:  Single-Ended Waveform								
		Positive Channel (p) = V <sub>IH</sub>								
		Negative Channel (n) = V <sub>IL</sub>								
R	Receiver Input Waveform									
		Differential Waveform (Mathematical Function of Positive & Negative Channel)								
		V <sub>ID</sub> 0 V								
		V <sub>ID</sub> p-n								
	Receiver input skew margin (RSKM)	High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = $(TUI - SW - TCCS) / 2$ .								
		V <sub>CCIO</sub> V <sub>OH</sub> V <sub>IH(AC)</sub>								
		V <sub>IH(DC)</sub>								
	Single-ended voltage- referenced I/O Standard	V <sub>IL(DC)</sub>								
S		V <sub>OL</sub>								
		The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform <i>ringing</i> .								
	SW (Sampling Window)	High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window								

Table 1-46. Glossary (Part 4 of 5)

ter	Term	Definitions							
	t <sub>C</sub>	High-speed receiver and transmitter input and output clock period.							
	Channel-to- channel-skew (TCCS)	High-speed I/O block: The timing difference between the fastest and slowest output edges, including $t_{\rm CO}$ variation and clock skew. The clock is included in the TCCS measurement.							
	t <sub>cin</sub>	Delay from the clock pad to the I/O input register.							
	t <sub>CO</sub>	Delay from the clock pad to the I/O output.							
	t <sub>cout</sub>	Delay from the clock pad to the I/O output register.							
	t <sub>DUTY</sub>	High-speed I/O block: Duty cycle on high-speed transmitter output clock.							
	t <sub>FALL</sub>	Signal high-to-low transition time (80–20%).							
	t <sub>H</sub>	Input register hold time.							
	Timing Unit Interval (TUI)	High-speed I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(Receiver\ Input\ Clock\ Frequency\ Multiplication\ Factor) = t_C/w).$							
	t <sub>INJITTER</sub>	Period jitter on the PLL clock input.							
	toutjitter_dedclk	Period jitter on the dedicated clock output driven by a PLL.							
	t <sub>OUTJITTER_IO</sub>	Period jitter on the general purpose I/O driven by a PLL.							
	t <sub>pllcin</sub>	Delay from the PLL inclk pad to the I/O input register.							
	t <sub>plicout</sub>	Delay from the PLL inclk pad to the I/O output register.							
	Transmitter Output Waveform	Standards:  Single-Ended Waveform  Positive Channel (p) = V <sub>OH</sub> Negative Channel (n) = V <sub>OL</sub> Ground  Differential Waveform (Mathematical Function of Positive & Negative Channel)  V <sub>OD</sub> 0 V  V <sub>OD</sub> p - n							
	t <sub>RISE</sub>	Signal low-to-high transition time (20–80%).  Input register setup time.							
	$t_{SU}$								

Letter	Term	Definitions
	V <sub>CM(DC)</sub>	DC common mode input voltage.
	V <sub>DIF(AC)</sub>	AC differential input voltage: The minimum AC input differential voltage required for switching.
	V <sub>DIF(DC)</sub>	DC differential input voltage: The minimum DC input differential voltage required for switching.
	V <sub>ICM</sub>	Input common mode voltage: The common mode of the differential signal at the receiver.
	V <sub>ID</sub>	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V <sub>IH</sub>	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	V <sub>IH(AC)</sub>	High-level AC input voltage.
	V <sub>IH(DC)</sub>	High-level DC input voltage.
	V <sub>IL</sub>	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	V <sub>IL (AC)</sub>	Low-level AC input voltage.
	V <sub>IL (DC)</sub>	Low-level DC input voltage.
	$V_{IN}$	DC input voltage.
	V <sub>OCM</sub>	Output common mode voltage: The common mode of the differential signal at the transmitter.
V	V <sub>OD</sub>	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} - V_{OL}$ .
	V <sub>OH</sub>	Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level.
	V <sub>OL</sub>	Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level.
	V <sub>OS</sub>	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$ .
	V <sub>OX (AC)</sub>	AC differential output cross point voltage: the voltage at which the differential output signals must cross.
	$V_{REF}$	Reference voltage for the SSTL and HSTL I/O standards.
	V <sub>REF (AC)</sub>	AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)} + noise$ . The peak-to-peak AC noise on $V_{REF}$ must not exceed 2% of $V_{REF(DC)}$ .
	V <sub>REF (DC)</sub>	DC input reference voltage for the SSTL and HSTL I/O standards.
	V <sub>SWING (AC)</sub>	AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	V <sub>SWING (DC)</sub>	DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	V <sub>TT</sub>	Termination voltage for the SSTL and HSTL I/O standards.
	V <sub>X (AC)</sub>	AC differential input cross point voltage: The voltage at which the differential input signals must cross.
W	_	_
X	_	_
Υ	_	_
Z	_	_

# **Document Revision History**

Table 1–47 lists the revision history for this chapter.

Table 1–47. Document Revision History

Date	Version	Changes
	1.5	<ul> <li>Updated "Maximum Allowed Overshoot or Undershoot Voltage", "Operating Conditions", and "PLL Specifications" sections.</li> </ul>
November 2011		■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21.
		■ Updated Figure 1–1.
		Updated for the Quartus II software version 10.1 release.
December 2010	1.4	■ Updated Table 1–21 and Table 1–25.
		<ul><li>Minor text edits.</li></ul>
		Updated for the Quartus II software version 10.0 release:
	1.3	■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45.
July 2010		■ Updated Figure 1–2 and Figure 1–3.
		<ul> <li>Removed SW Requirement and TCCS for Cyclone IV Devices tables.</li> </ul>
		Minor text edits.
		Updated to include automotive devices:
		<ul><li>Updated the "Operating Conditions" and "PLL Specifications" sections.</li></ul>
March 2010	1.2	■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43.
		<ul> <li>Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os.</li> </ul>
		<ul> <li>Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.</li> </ul>
		Minor text edits.
February 2010	1.1	<ul> <li>Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release.</li> </ul>
		Minor text edits.
November 2009	1.0	Initial release.