TEXAS INSTRUMENTS

TWL92230

ENERGY MANAGEMENT DEVICE COMPANION DEVICE FOR THE OMAP24xx

Data Manual

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1 Introduction

The TWL92230 is an energy management device optimized to be a companion device for the OMAP24xx application processor. It contains power supplies and reference voltage for OMAP24xx (V_{CORE}, V_{IO}, V_{ADAC}, V_{PLL}, and a 0.5-V reference), for associated memory (V_{MEM}), for two independently powered memory cards (V_{MCS1} and V_{MCS2}) and also for an extra device or auxiliary peripheral (V_{AUX}). It contains all relevant interface signals to OMAP24xx, that allow monitoring, operation control, and changing of regulator voltage settings via the I^2C serial interface. The TWL92230 also has memory card transceivers to adapt a 1.8-V processor I/O voltage to the memory card voltages. It supports two slots for MMC, SDIO, SD, or Memory Stick cards.

The TWL92230 is housed in an 80-terminal, lead-free (Pb, atomic number 82), MicroStar^{TM} BGA package (ZQE), and is fabricated with the 3370A07S process (an advanced BiCMOS process customized for MS wireless products).

1.1 Features

- An 880-mA buck dc-dc converter for processor core (V_{OUT} = 1.00 V to 1.45 V).
- Two 400-mA buck dc-dc converters (V_{OUT} = 1.5 V to 3.2 V). One dc-dc converter can be used as a preregulator for the VIO and the VMEM LDO regulators. The other dc-dc converter can power a high-current Memory Card slot.
- The dc-dc converters run at 1.2 MHz, provided by an internal clock or the clock generator/divider that accepts 12 MHz, 13 MHz, or 19.2 MHz as the high-frequency clock input.
- One 200-mA LDO regulators (V_{OUT} = 1.50 V, 1.80 V, 1.90 V, or 2.50 V). It typically powers memory.
- One 200-mA LDO regulator (V_{OUT} = 1.85 V, 2.80 V, 3.00 V, or 3.10 V). It typically powers a Memory Card slot, MMC/SD slot 1 (high-current level compliant with MMC/SD and SDIO 1.0).
- Two 200-mA LDO regulator (V_{OUT} = 1.50 V, 1.80 V, 2.50 V, or 2.80 V). They typically power an extra device (flash memory, SDRAM, peripheral, etc.) and the processor I/O.
- One 10-mA, high-PSRR, low-noise LDO regulator (1.30 V). It typically powers the processor PLL.
- One 2-mA, high-PSRR, low-noise LDO regulator (1.80 V). It typically powers the processor TV-Out DAC.
- One 0.5-V voltage reference that typically powers the processor TV-Out DAC.
- Backup battery switch provides the input voltage for the low-current VDIG LDO regulator. The output of this LDO is externally available for connection to a filter capacitor, but it must not be loaded externally.
- Allows dynamic voltage management for the processor core voltage.
- 32-kHz oscillator and integrated real-time clock (RTC). An external crystal or a digital 32-kHz clock signal is required.
- 400 kHz I^2C compatible serial interface.
- Three general-purpose I/O ports (GPIOs). Some GPIOs may have alternative functions.
- Dual slot memory card transceivers that can be powered independently.
- Monitoring and detection circuits: thermal shutdown, hot die, low-battery, and undervoltage lockout.
- Housed in a 5mm × 5mm package (80ZQE) that is RoHS compliant and lead-free soldering process compatible.
- Typical applications: Cellular phones, smartphones, and PDAs

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1.2 Overall Description and Block Diagram

Figure 1−1 shows the TWL92230 block diagram. The major blocks are the reference system (with main bandgap and a 0.5-V voltage reference), clock generation system, I^2C serial interface, Memory Card transceivers, digital control system, power supply module (containing three dc-dc converters and seven LDO regulators), battery switch, and monitoring system.

All controlling and sequencing are performed by the digital control system according to its state machine, monitoring inputs, and commands via the I^2C serial interface. The reference system provides the bandgap voltage and bias currents required for the blocks. Enable/disable signals on each block allow the bias currents to be shutdown whenever necessary (for instance, during an inactive state).

In the clock generation system there is a 32-kHz oscillator, a real-time clock (RTC) circuit, and a clock divider for the high-frequency clock input. This oscillator generates a clock that is used internally for synchronization and by the RTC to maintain the date when the processor is completely shutdown. This 32-kHz clock is also available externally for the OMAP24xx (and other devices that may require it). The TWL92230 can use a high-frequency clock input (HFCLK), or it can use the internal RC oscillator. This clock is divided inside the clock generation system allowing a 1.2-MHz clock to be delivered to the dc-dc converters.

Analog circuits are powered by VBAT, and they are assured to be fully functional for VBAT equal to or higher than 2.4 V, unless stated otherwise. Analog circuits are parametric compliant for VBAT equal to or higher than 2.8 V, unless stated otherwise. Internal digital power supply is DVDD and is provided by the VDIG LDO regulator (1.8 V typical). Digital circuits powered by DVDD are assured operational for voltage down to 1.7 V. IO_1P8 terminal should be externally wired to a regulated supply with 1.8-V output voltage (such as VIO or DCDC2 regulators)

All blocks can be enabled and operational during normal mode, but all nonessential circuits are disabled during M_NoPower, M_WaitON and M_Backup states, in order to minimize current consumption. The essential circuits that are always operational (for VBAT > 2.4 V or BAKB > 2.4 V) have very low-power consumption. The TWL92230 must be turned off when battery voltage goes below the Low-Bat falling threshold.

The TWL92230 has five different system states that are described in section 10.7, *System States and State Machine Sequencer*.

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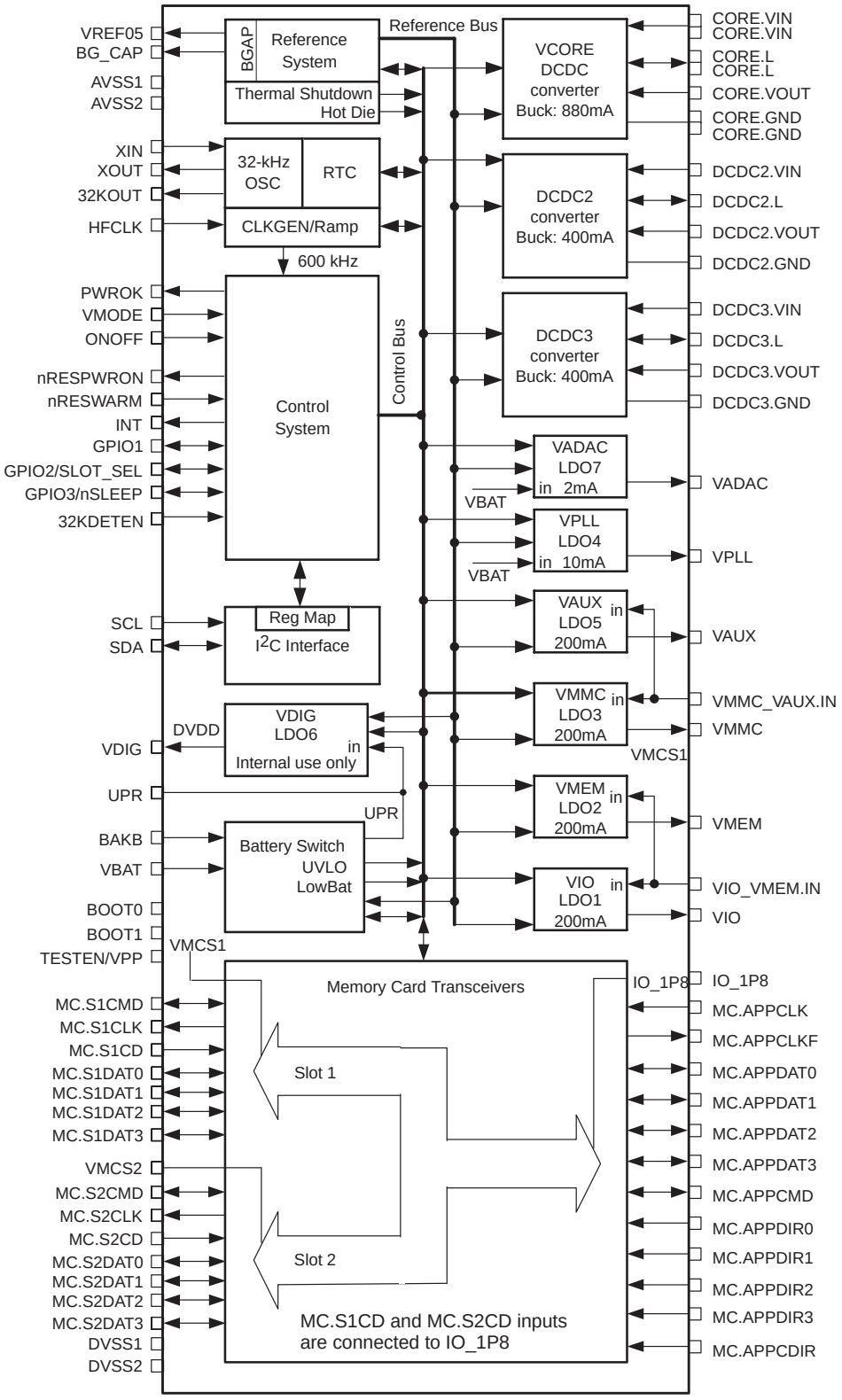


Figure 1−1. TWL92230 Functional Block Diagram

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1.3 Terminal Descriptions

Table 1−1. Terminal Descriptions

TERMINAL		ABSMAX (V)	SIGNAL TYPE(1)	DESCRIPTION
NAME	NO.			
BG_CAP	J4	−0.3 to 1.0	In/Out A	For external bandgap capacitor
AVSS2	H5	−0.3 to 0.3	Ground	Primary analog ground
XIN	E1	−0.3 to 2.5	In A	32-kHz crystal oscillator input or bypass input
XOUT	F2	−0.3 to 2.5	Out A	32-kHz crystal oscillator output
32KOUT	E3	−0.3 to 2.1	Out D	32-kHz clock digital output
HFCLK	D3	−0.3 to 2.1	In D	High-frequency clock input
PWROK / SCAN_OUT	H7	−0.3 to 2.1	Out D	VCORE power stable output. SCAN_OUT when SCAN_MODE=1
VMODE / SCAN_EN	G3	−0.3 to 2.1	In D	Synchronization input signal for VCORE voltage scaling. SCAN_EN when SCAN_MODE=1
ONOFF	J7	−0.3 to 5.5	In D	On-Off signal input or pushbutton input
nRESPWRON	F4	−0.3 to 2.1	Out D	Power-on reset output to the Application Processor
nRESWARM	H3	−0.3 to 2.1	In D	Warm reset to application processor and/or peripherals
INT	E4	−0.3 to 2.1	Out D	Interrupt output signal
GPIO1	G6	−0.3 to 2.1	In/Out 3S D	General-purpose Input/Output 1
GPIO2 / SLOT_SEL	H4	−0.3 to 2.1	In/Out 3S D	General-purpose Input/Output 2 / Slot selection Input
GPIO3/ nSLEEP_EN	G4	−0.3 to 2.1	In/Out 3S D	General-purpose Input/Output 3 / Sleep Enable State
IO_1P8	A3	−0.3 to 2.1	Power	Power supply for I/Os. Typically wired to VIO (or DCDC2)
SCL / SCAN_CLK	D4	−0.3 to 2.1	In D	Serial interface clock input. SCAN_CLK when SCAN_MODE=1
SDA / SCAN_IN	D5	−0.3 to 2.1	In/Out D	Serial interface data input/output. SCAN_IN when SCAN_MODE = 1
32KDETEN	J3	−0.3 to 2.1	In A	32-kHz detect enable
VDIG	J5	−0.3 to 2.1	Out A	VDIG output voltage
UPR	H6	−0.3 to 5.5	In/Out A	Battery switch output
BAKB	G5	−0.3 to 5.5	In/Out A	Backup battery input
VBAT	J6	−0.3 to 5.5	Power	Main battery input
BOOT0 / TESTOUT0	E5	−0.3 to 5.5	In/Out A	Configuration input for Startup Mode (TESTEN=0). TESTOUT0 is used for analog testability (TESTEN=1)
TESTEN/VPP	G7	−0.3 to 14	HV In D	Used for test enabled or to program EEPROM bits
BOOT1 / TESTOUT1	F5	−0.3 to 5.5	In/Out A	Configuration input for the Startup Mode (TESTEN=0). TESTOUT1 is used for analog testability (TESTEN=1)
MC.S1CMD	E7	−0.3 to 3.4	In/Out D	Command signal for Memory Card in slot1
MC.S1CLK	E8	−0.3 to 3.4	Out D	Clock signal for Memory Card in slot1
MC.S1CD	D6	−0.3 to 2.1	In D	Card Detect signal for Memory Card in slot1
MC.S1DAT0	E9	−0.3 to 3.4	In/Out D	Data bit0 for Memory Card in slot1
MC.S1DAT1	F6	−0.3 to 3.4	In/Out D	Data bit1 for Memory Card in slot1
MC.S1DAT2	D8	−0.3 to 3.4	In/Out D	Data bit2 for Memory Card in slot1
MC.S1DAT3	D9	−0.3 to 3.4	In/Out D	Data bit3 for Memory Card in slot1
VMCS2	A9	−0.3 to 3.4	Power	Memory Card voltage supply, slot2
MC.S2CMD	C7	−0.3 to 3.4	In/Out D	Command signal for Memory Card in slot2
MC.S2CLK	C8	−0.3 to 3.4	Out D	Clock signal for Memory Card in slot2
MC.S2CD	E6	−0.3 to 2.1	In D	Card Detect signal for Memory Card in slot2

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Table 1−1. Terminal Descriptions (Continued)

TERMINAL		ABSMAX (V)	SIGNAL TYPE(1)	DESCRIPTION
NAME	NO.			
MC.S2DAT0	C9	−0.3 to 3.4	In/Out D	Data bit0 for Memory Card in slot2
MC.S2DAT1	D7	−0.3 to 3.4	In/Out D	Data bit1 for Memory Card in slot2
MC.S2DAT2	B8	−0.3 to 3.4	In/Out D	Data bit2 for Memory Card in slot2
MC.S2DAT3	B9	−0.3 to 3.4	In/Out D	Data bit3 for Memory Card in slot2
CORE.VIN	A2	−0.3 to 5.5	Power	Input voltage for VCORE
CORE.VIN	A1	−0.3 to 5.5	Power	Input voltage for VCORE
CORE.L	B2	−0.3 to 5.5	Out A	Switch output of VCORE (to be connected to inductor)
CORE.L	B1	−0.3 to 5.5	Out A	Switch output of VCORE (to be connected to inductor)
CORE.VOUT	D2	−0.3 to 1.8	In A	VCORE feedback voltage sense input
CORE.GND	C2	−0.3 to 0.3	Ground	Power ground for VCORE
CORE.GND	C1	−0.3 to 0.3	Ground	Power ground for VCORE
DCDC2.VIN	J2	−0.3 to 5.5	Power	Input voltage for DCDC2
DCDC2.L	J1	−0.3 to 5.5	Out A	Switch output of DCDC2 (to be connected to inductor)
DCDC2.VOUT	H2	−0.3 to 3.4	In A	DCDC2 feedback voltage sense input
DCDC2.GND	H1	−0.3 to 0.3	Ground	Power ground for DCDC2
DCDC3.VIN	J8	−0.3 to 5.5	Power	Input voltage for DCDC3
DCDC3.L	J9	−0.3 to 5.5	Out A	Switch output of DCDC3 (to be connected to inductor)
DCDC3.VOUT	H8	−0.3 to 3.4	In A	DCDC3 feedback voltage sense input
DCDC3.GND	H9	−0.3 to 0.3	Ground	Power ground for DCDC3
VPLL	E2	−0.3 to 1.6	Out A	VPLL output voltage
VMMC_VAUX.IN	G9	−0.3 to 5.5	Power	Input voltage for VMMC and VAUX LDOs
VAUX	G8	−0.3 to 3.1	Out A	VAUX output voltage
VREF05	F8	−0.3 to 1.0	In/Out A	For external 0.5-V reference and VREF05 capacitor
VMMC	F9	−0.3 to 3.3	Out A	VMMC output voltage
VIO_VMEM.IN	G1	−0.3 to 5.5	Power	Input voltage for VIO and VMEM LDOs
VMEM	G2	−0.3 to 2.8	Out A	VMEM output voltage
VADAC	D1	−0.3 to 2.1	Out A	VADAC output voltage
VIO	F1	−0.3 to 3.1	Out A	VIO output voltage
MC.APPCLK	C4	−0.3 to 2.1	In D	Clock input for Memory Card Interface
MC.APPCLKF	A4	−0.3 to 2.1	Out D	Clock output feedback for Memory Card Interface
MC.APPDAT0	C5	−0.3 to 2.1	In/Out D	Data input/output 0 for Memory Card Interface
MC.APPDAT1	B3	−0.3 to 2.1	In/Out D	Data input/output 1 for Memory Card Interface
MC.APPDAT2	A7	−0.3 to 2.1	In/Out D	Data input/output 2 for Memory Card Interface
MC.APPDAT3	B7	−0.3 to 2.1	In/Out D	Data input/output 3 for Memory Card Interface
MC.APPCMD	B4	−0.3 to 2.1	In/Out D	Command input/output for Memory Card Interface
MC.APPDIR0	A6	−0.3 to 2.1	In D	Direction for data input 0 for Memory Card Interface
MC.APPDIR1	C6	−0.3 to 2.1	In D	Direction for data input 1 for Memory Card Interface
MC.APPDIR2	B5	−0.3 to 2.1	In D	Direction for data input 2 for Memory Card Interface
MC.APPDIR3	B6	−0.3 to 2.1	In D	Direction for data input 3 for Memory Card Interface
MC.APPCDIR	A5	−0.3 to 2.1	In D	Direction for command for Memory Card Interface
DVSS1	F7	−0.3 to 0.3	Ground	Digital ground
DVSS2	A8	−0.3 to 0.3	Ground	Digital ground
AVSS1	F3	−0.3 to 0.3	Ground	Dedicated analog ground for REFSYS and 32-kHz oscillator

(1) In = Input, Out = Output, 3S = Tri-State, OD = Open-Drain, PU = Pullup, PD = Pulldown, A = Analog, D = Digital

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2 Electrical Information

2.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under section 2.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 2−1. Absolute Maximum Ratings

PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
Main battery supply voltage	Typically Li-Ion or Li-Polymer cell battery	−0.3	5.5	V
Voltage on any input	Where supply represents the voltage applied to the power-supply pin associated with the input	−0.3	Supply+0.3	V
Storage temperature range		–55	125	°C
Ambient temperature range		–30	85	°C
Junction temperature (T_j)			150(1)	°C
Junction temperature (T_j) for parametric compliance		−30	125	°C

(1) This temperature can shortly rise above this value during the thermal shutdown event.

2.2 Recommended Operating Conditions

Specifications found throughout this document apply over the following recommended operating conditions, unless noted otherwise:

Table 2−2. Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS
Ambient temperature range	–30		85	°C
Main battery supply voltage (VBAT)	2.8	3.6	4.5	V
Backup battery supply voltage (BAKB)	2.4	3.2	4.5	V
CORE_VIN power input	2.8	VBAT	4.5	V
DCDC2.VIN power input	2.8	VBAT	4.5	V
DCDC3.VIN power input	2.8	VBAT	4.5	V
VIO.IN power input VMEM.IN power input	2.0	DCDC2	4.5	V
VMMC.IN power input VAUX.IN power input	2.0	VBAT	4.5	V
VDIG.IN power input (internal)	2.4	UPR	4.5	V
Input/Output MCS1DAT[3:0] Input/Output MCS1CMD V_{MCS1} power input	1.7	VMMC	3.3	V
Input/Output MCS2DAT[3:0] Input/Output MCS2CMD V_{MCS2} power input	1.7	DCDC3	3.3	V
Input/Output MCAPPDAT[3:0] Input/Output MCAPPCMD Input MCAPPCLK Input MCAPPDIR[3:0] Input MCAPPCDIR	1.7	IO_1P8	1.9	V
IO_1P8 power input	1.7	VIO	1.9	V

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2.3 Electrical Characteristics

Table 2−3 shows the generic electrical characteristics of the TWL92230 for the following conditions: VBAT = 2.8 V to 4.5 V, $T_{AMBIENT}$ = −30°C to 85°C

Table 2−3. Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IH}	Input high-voltage(1)		$0.7\times V_{IO_1P8}$	$V_{IO_1P8}+0.3$	V
V_{IL}	Input low-voltage(1)		−0.3	$0.3\times V_{IO_1P8}$	V
V_{IH}	Input high-voltage(2)		0.7 × VDIG	VDIG + 0.3	V
V_{IL}	Input low-voltage(2)		−0.3	0.3 × VDIG	V
V_{IH}	Input high-voltage(3)		0.7 × VDIG	VDIG + 0.3	V
V_{IL}	Input low-voltage(3)		−0.3	0.3 × VDIG	V
V_{OH}	Output high-voltage(4)	I_{OH} = −100 µA at V_{IO_1P8} min	$V_{IO_1P8}-0.2$		V
V_{OL}	Output low-voltage(4)	I_{OL} = 100 µA at V_{IO_1P8} min		0.2	V
V_{IH}	Input high-voltage(6)	1.7 V to 1.95 V	$V_{MCS}\times 0.70$	V_{MCS} + 0.2	V
		1.95 V to 2.7 V	1.7	V_{MCS} + 0.2	
		2.7 V to 3.2 V	2	V_{MCS} + 0.2	
V_{IL}	Input low-voltage(6)	1.7 V to 1.95 V	−0.3V	$V_{MCS}\times 0.30$	V
		1.95 V to 2.7 V	−0.3V	0.7	
		2.7 V to 3.2 V	−0.3V	0.8	
V_{IH}	Input high-voltage(8)		0.7 × V_{UPR}	V_{UPR} + 0.3	V
V_{IL}	Input low-voltage(8)		−0.3	0.3 × V_{UPR}	V
V_{IH}	Input high-voltage(9)		0.7 × V_{DIG}	V_{BAT} + 0.3	V
V_{IL}	Input low-voltage(9)		−0.3	0.3 × V_{DIG}	V
t_{tr}	Input rise/fall time(1)	10% to 90% or 90% to 10%		25	ns
t_{tr}	Input rise/fall time(2)	10% to 90% or 90% to 10%		40	ns
C_{PIN}	Input capacitance(1)(8)			10	pF
I_{LEAK}	Pin leakage current(1)	$0 < V_{IN} < V_{IO_1P8}$	−1	1	µA
I_{LEAK}	Pin leakage current(2)	$0 < V_{IN} <$ VDIG	−1	1	µA
I_{LEAK}	Pin leakage current(6)	$0 < V_{IN} <$ VMCSx	−1	1	µA
V_{OH}	Output high-voltage(5)	I_{OH} = 1 mA	$0.8\times V_{IO_1P8}$	V_{IO_1P8}	V
V_{OL}	Output low-voltage(5)	I_{OL} = 1 mA		$0.2\times V_{IO_1P8}$	V
V_{OH}	Output high-voltage(7)	I_{OH} = −100 µA @ V_{MCS} min	V_{MCS} − 0.2		V
V_{OL}	Output low-voltage(7)	I_{OL} = 100 µA @ V_{MCS} min		0.2	V

(1) Specification applies to the following pins: VMODE, GPIO[3:1], SCL, SDA, MCAPPCLK, MCAPPDAT[3:0], MCAPP-DIR[3:0], MCAPPCMD and HFCLK (this terminal is fail-safe)
(2) Specification applies to the 32-kHz clock source, when a crystal is not used. In this case an external series resistor (100K) is connected between XIN terminal and this clock source.
(3) Specification applies to the 32KDETEN pin.
(4) Specification applies to the following pins: MCAPPCLKF, MCAPPDAT[3:0], and MCAPPCMD.
(5) Specification applies to the following pins: 32KOUT, PWROK, nRESPWRON, RESWARM, INT, GPIO[4:1], SDA
(6) Specification applies to the following pins: MC.S1CMD, MC.S1DAT[3:0], MC.S2CMD and MC.S2DAT[3:0].
(7) Specification applies to the following pins: MC.S1CMD, MC.S1CLK, MC.S1DAT[3:0], MC.S2CMD, MC.S2CLK and MC.S2DAT[3:0].
(8) Specification applies to the following pins: BOOT0, BOOT1
(9) Specification applies to the following pins: ONOFF

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2.4 Current Consumption

Table 2−4 shows the generic electrical characteristics for the TWL92230 for the following conditions: VBAT = 3.6 V, $T_{AMBIENT}$ = −30°C to 85°C

Table 2−4. Current Consumption

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
ICC1	M_WaitOn State Current Consumption	All dc-dc converters and LDOs (except VDIG) are OFF. Reference System is ON. Clock System is OFF. Memory Card Transceivers are OFF.		70	µA
ICC2	M_Active State Current Consumption, Typical Configuration 0	VCORE and DCDC2 converters, and the VIO, VMEM and VPLL LDOs are in sleep mode. DCDC3 converter, VMMC, VAUX and VADAC LDOs are OFF. Reference System is ON. Clock System is ON. Memory Card Transceivers are OFF.		300	µA
ICC3	M_Active State Current Consumption, Typical Configuration 3	VCORE and DCDC2 converters and the VPLL LDO are in sleep mode. DCDC3 converter and the VIO, VMEM, VMMC, VAUX and VADAC LDOs are OFF. Reference System is ON. Clock System is ON. Memory Card Transceivers are OFF.		300	µA
ICC4	M_Active_State Current Consumption, No Load dc-dc & LDO are in Sleep mode with no load	VCORE, DCDC2., DCDC3, VIO, VMEM, VMMC, VAUX, VPLL are in sleep mode with zero load. Reference System is ON. Clock System is ON. Memory Card Transceivers are OFF.		400	µA
ICC5	M_Active_State Current Consumption, No Load dc-dc & LDO are in On mode with no load	VCORE, DCDC2., DCDC3, VIO, VMEM, VMMC, VAUX, VPLL & VADAC are in active mode with zero load. Reference System is ON. Clock System is ON. Memory Card Transceivers are ON.		800	µA

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2.5 ESD Performance

The TWL92230 device meets Texas Instruments standard requirements relative to the electrostatic discharge (ESD) sensitivity. The following list details the TWL92230 ESD performance relative to TI requirements:

Table 2−5. ESD Performance

ESD METHOD	STANDARD REFERENCE	TWL92230 PERFORMANCE	TI STANDARD REQUIREMENTS
Human body model	JESD22-A114-B	2000 V	2000 V
Machine model	JESD22-A115-A	100 V	100 V
Charge device model	JESD22-C101B.01	500 V	500 V

3 Switch Mode Power Supplies (SMPS)

The TWL92230 contains three switch-mode power supplies:

- One 880-mA, buck dc-dc converter for the processor core (V_{OUT} = 1.00 V to 1.45 V).
- One 400-mA, buck dc-dc converter (V_{OUT} = 1.5 V to 3.2 V), that is typically used as a preregulator for the VIO and the VMEM LDO regulators.
- One 400-mA, buck dc-dc converter (V_{OUT} = 1.5 V to 3.2 V), that typically powers the MMC/SD slot 2 (high-current level compliant with MMC/SD and SDIO 1.0).

The power-up default clock source for the dc-dc converters is an integrated RC oscillator output with a nominal switching frequency of the converter of 1.2 MHz. Alternatively the clock applied to the HFCLK terminal can be used as the clock source. This is better described in section 6, *Clock Generation System*.

The typical Rds_on is 0.7 Ω at 400 mA.

Figure 3−1 shows the block diagram of these buck dc-dc converters connected to typical external components.

All dc-dc converter input voltage terminals are recommended to have a 22-µF capacitor (X5R or X7R).

All DCDC2.VIN, DCDC2.VOUT, DCDC2.L, and DCDC2.GND pins should be grounded when DCDC2 is not in use.

All DCDC3.VIN, DCDC3.VOUT, DCDC3.L, and DCDC3.GND pins should be grounded when DCDC3 is not in use.

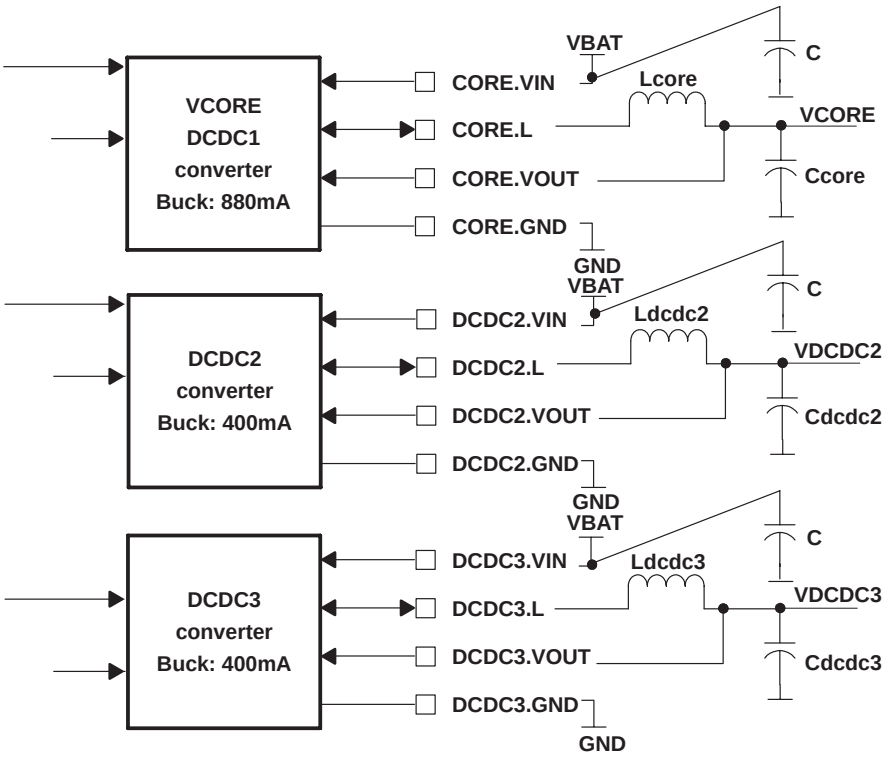


Figure 3−1. Switch Mode Power Supplies and External Connections

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The VCORE buck converter is designed for three modes of operation.

Table 3−1. VCORE Modes of Operation

MODE	VCORE_MODE[1:0]	V_{OUT} (NOMINAL)	I_{OUT} (MAX)
Off	00	0	0
Sleep	01	Per Setting	Design Rating
Reserved	10	Per Setting	Design Rating
ON_PWM	11	Per Setting	Design Rating

The DCDC2 and DCDC3 buck converters are designed for three modes of operation.

Table 3−2. DCDC2 and DCDC3 Modes of Operation

MODE	DCDCX_MODE[2:0]	V_{OUT} (NOMINAL)	I_{OUT} (MAX)
Off	000	0	0
Reserved	1xx		
Sleep	001	Per Setting	Design Rating
Reserved	010		
ON_PWM	011	Per Setting	Design Rating

The off mode of operation shuts down the dc-dc converter and always results in V_{OUT} = 0 V and I_{OUT} = 0 A.

The sleep mode uses pulse frequency modulation (PFM). In this burst mode a higher efficiency can be achieved, but more ripple is present and the dc-dc converter is unable to drive heavy loads in this mode of operation.

The ON_PWM mode selects normal dc-dc converter operation but limits the converter to PWM timing. The ON_PWM has a discontinuous mode (pulse skipping) for low currents and a continuous mode (PWM) for higher currents. At low output currents, this ON_PWM mode (in pulse skipping) can be less efficient than the PFM Burst mode (sleep mode), but will have lower ripple and therefore smaller switching noise. At higher output currents, this ON_PWM mode can generate predictable switching noise that may cause less interference for the RF components in the system, if the clock source in this mode is the signal at pin HFCLK and chosen so that the switching frequency of the converter can be tied to the RF reference source. If this mode is selected, but a clock is not provided on HFCLK, then the internal mux selects the internal oscillator that will provide the clock, but the switching noise is not predictable.

These buck converters have soft-start for smooth startup during the power-up.

3.1 VCORE DCDC1 Converter

VCORE is a programmable, synchronous buck switch converter having internal switch MOSFETs. The external inductor and capacitor are optimized for 1.2-MHz operation. The processor can force it into a sleep mode that improves efficiency under light load conditions. Table 3−3 shows the default configuration of VCORE register bits for each system state. A soft-start circuit limits the inrush current.

See section 10.1.3 and Appendix A for additional VMODE operation and Digital Voltage Scaling implementation, respectively.

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Table 3−3. VCORE DCDC1 Converter Electrical Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage (V_{IN})			2.8	V_{IN}	4.5	V
Output voltage	On mode: VCORE_MODE[1:0] = 11, 2.8 V < V_{IN} < 4.5 V, 0 mA < I_O < I_{max} or Sleep mode: VCORE_MODE[1:0] = 01, 2.8 V < V_{IN} < 4.5 V, 0 mA < I_O < 20 mA	VCORE_VOLT[4:0] = 00000		1.000		V
		VCORE_VOLT [4:0] = 00001		1.025		
		VCORE_VOLT [4:0] = 00010		1.050		
		VCORE_VOLT [4:0] = 00011		1.075		
		VCORE_VOLT [4:0] = 00100		1.100		
		VCORE_VOLT [4:0] = 00101		1.125		
		VCORE_VOLT [4:0] = 00110		1.150		
		VCORE_VOLT [4:0] = 00111		1.175		
		VCORE_VOLT [4:0] = 01000		1.200		
		VCORE_VOLT [4:0] = 01001		1.225		
		VCORE_VOLT [4:0] = 01010		1.250		
		VCORE_VOLT [4:0] = 01011		1.275		
		VCORE_VOLT [4:0] = 01100		**1.300**		
		VCORE_VOLT [4:0] = 01101		1.325		
		VCORE_VOLT [4:0] = 01110		1.350		
		VCORE_VOLT [4:0] = 01111		1.375		
		VCORE_VOLT [4:0] = 10000		1.400		
		VCORE_VOLT [4:0] = 10001		1.425		
		VCORE_VOLT [4:0] = 10010		1.450		
Output voltage accuracy	Inc. ripple, dc and transient line and load regulations For maximum slew rate of 80 mA/µs at the output		−4.7		5.2	%
Ground current (I_Q)	Off mode (at 85°C): VCORE_MODE[1:0] = 00				1	µA
	Sleep mode: VCORE_MODE[1:0] = 01, I_O = 0 mA, 1.2 MHz				40	
	On mode: VCORE_MODE[1:0] = 11, I_O = 0 mA, 1.2 MHz				120	
Output current (I_{MAX}), sleep mode	1.0 V < V_{OUT} < 1.3 V				20	mA
Output current (I_{MAX}), ON mode	V_{OUT} = 1.05 V				440	mA
Output current (I_{MAX}), ON mode	V_{OUT} > 1.30 V				880	mA
Short circuit current (I_{OS})	V_{IN} = V_{MAX}		1200		Survival guaranteed	mA
Filter capacitance (C_L)	X5R or X7R		11	22	33(2)	µF
ESR of capacitor (R_{esr}, including parasitic resistances from PWB)	f = 1.2 MHz		2		50	mΩ
Filter coil inductance			3.29	4.70	6.11	µH
Filter coil dc maximum resistance					125(1)	mΩ
Coil saturation current	Based on 30% inductance reduction from typical value		1100			mA
Soft start current				350		mA
Load regulation	0 < I_O < I_{MAX}, V_{OUT} = 1.3 V			40		mV
Line regulation	V_{OUT} = 1.3 V			20		mV
Ripple, On mode	V_{OUT} = 1.3 V			10		mV

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Table 3−3. VCORE DCDC1 Converter Electrical Characteristics (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ripple, Sleep mode	V_{OUT} = 1.3 V		10		mV
Transient load regulation	I_O = 1 to 250 mA in Max slew = 80 mA/µs I_O = 200 to 400 mA in Max slew = 80 mA/µs		10		mV
Transient line regulation	300 mVpp ac square wave, with 10-µs rise/fall times		5		mV
$t_{RECOVERY}$ (Sleep to On mode or On to Sleep mode)	In Sleep: I_O = 5 mA, V_{IN} = V_{BAT} =2.8 V, In On: I_O = 100 mA, V_{IN} = V_{BAT} =2.8 V		30	50	µs
t_{ON}, OFF to ON	I_O = 0, C_L = 22 µF (within 5% of V_{OUT})		100	500	µs
$t_{1.05V\text{-}to\text{-}1.30V}$	I_O = 300 mA max in Normal mode, I_O = 5 mA max in Sleep mode			100	µs
$t_{1.05V\text{-}to\text{-}1.40V}$	I_O = 20 mA in Sleep Mode to <300 mA in Normal mode, STEP_nJMP = BYP_COMP = VCSLPEN1 = 1, STEP_PER = 0			100	µs
t_{OFF}	V_{OUT} < 0.5 V			10	ms
Output shunt (pulldown) resistance	I_O = 1 µA		70		Ω
Overshoot	Off to On, I_O = 0			3	%
Pulse Skipping mode threshold	V_{OUT} = 1.3V, V_{BAT} = 2.8V		40		mA
Conversion efficiency, On mode	I_O = 10 mA, V_{OUT} = 1.3 V		80		%
	I_O = 200 mA, V_{OUT} = 1.3 V		86		
	I_O = 720 mA, V_{OUT} = 1.3 V		80		
	I_O = 880 mA, V_{OUT} = 1.3 V		78		
Conversion efficiency, Sleep mode	I_O = 20 mA, V_{OUT} = 1.3 V		85		%
Switching frequency			1200		kHz

All specifications are for default values only (in **bold**), unless stated otherwise.

(1) Filter coil dc max resistance can go up to 200 mΩ but conversion efficiency will decrease.

(2) Up to 20-µF low-ESR (<50 mΩ) capacitance can be placed in parallel to the Filter capacitor (C_L) without compromising the stability; however, specification values above may change

(3) Maximum allowed value is 0x12. Any attempt to write a value higher than the maximum will result in 0x12 being written, instead.

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3.2 DCDC2 DC-DC Converter

DCDC2 is a programmable, synchronous buck switch converter having internal switch MOSFETs. The external inductor and capacitor are optimized for 1.2-MHz operation. The processor can force it into a sleep mode that improves efficiency under light load conditions. Table 3−4 shows the default configuration of DCDC2 register bits for each system state. A soft start circuit limits the inrush current.

Table 3−4. DCDC2 DC-DC Converter Electrical Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage (V_{IN})			2.8	V_{IN}	4.5	V
Output voltage (V_{OUT})	On mode: DCDC2_MODE[2:0] = 011, V_{OUT} + 0.6 V < V_{IN} < 4.5 V, 0 mA < I_O < 400 mA or Sleep mode: DCDC2_MODE[2:0] = 001, V_{OUT} + 0.6 V < V_{IN} < 4.5 V, See Output current for I_{MAX} rating.	DCDC2_VOLT [2:0] = 000		1.5		V
		DCDC2_VOLT [2:0] = 001		**1.8**(1)		
		DCDC2_VOLT [2:0] = 010		2.0		
		DCDC2_VOLT [2:0] = 011		**2.2**(2)		
		DCDC2_VOLT [2:0] = 100		2.4		
		DCDC2_VOLT [2:0] = 101		2.8		
		DCDC2_VOLT [2:0] = 110		3.0		
		DCDC2_VOLT [2:0] = 111		3.2		
Output voltage accuracy	Inc. ripple, dc and transient line and load regulations For maximum slew rate of 40 mA/µs at the output		−5		+5	%
Output voltage accuracy	Inc. ripple, dc line and load regulations (without transient regulation)			3		%
Ground current (I_Q)	Off mode (at 85°C): DCDC2_MODE[2:0] = 000				1	µA
	Sleep mode: DCDC2_MODE[2:0] = 001, I_O = 0 mA max, 1.2 MHz				40	
	On mode: DCDC2_MODE[2:0] = 011, I_O = 0 mA max, 1.2 MHz				120	
Output current (I_{MAX}), Sleep mode	V_{OUT} = 1.5 to 1.8 V				10	mA
	V_{OUT} = 2.0 to 2.8 V				5	
	V_{OUT} = 3.0 V				2	
	V_{OUT} = 3.2 V				1	
Output current (I_{MAX}), On mode					400	mA
Short circuit current (I_{OS})	V_{IN} = V_{MAX}		700		Survival guaranteed	mA
Filter capacitor (C_L)	X5R or X7R		11	22	33(5)	µF
ESR of capacitor (R_{ESR})	f = 1.2 MHz		2		50	mΩ
Filter coil inductance			3.29	4.70	6.11	µH
Filter coil dc max resistance					125(3)	mΩ
Coil saturation current	Based on 30% inductance reduction from typical value		700			mA
Soft Start current				190		mA
Load regulation	0 < I_O < I_{MAX}, V_{OUT} = 2.2 V			35		mV
Line regulation	V_{OUT} = 2.2 V			25		mV
Transient load regulation	I_O = 0 to I_{MAX}, V_{OUT} = 2.2 V, Max slew = 40 mA/µs			12		mV
Transient line regulation	300 mVpp ac square wave, with 10-µs rise/fall times, V_{OUT} = 2.2 V			5		mV
$t_{RECOVERY}$ (Sleep to On mode or On to Sleep mode)	In Sleep: I_O = 5 mA, V_{IN} = V_{BAT} =2.8 V In On: I_O = 100 mA, V_{IN} = V_{BAT} =2.8 V			30	50	µs
t_{ON}, Off to On	I_O = 0, C_L = 22 µF (within 5% of V_{OUT})			450	600	µs
t_{OFF}	V_{OUT} < 0.5 V				10	ms

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Table 3−4. DCDC2 DC-DC Converter Electrical Characteristics (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output shunt (pulldown) resistance	I_O = 1 µA		70		Ω
Overshoot	Off to On, I_O = 0			3	%
Conversion efficiency, On mode	I_O = 10 mA, V_{OUT} = 1.8 V, 2.2 V		75		%
	I_O = 100 mA, V_{OUT} = 1.8 V, 2.2 V		85		
	I_O = 400 mA, V_{OUT} = 1.8 V, 2.2 V		85		
Conversion efficiency, Sleep mode	I_O = 10 mA, V_{OUT} = 1.8 V		85		%
	I_O = 5 mA, V_{OUT} = 2.2 V		88(5)		
Switching frequency			1200		kHz

All specifications are for default values only (in **bold**), unless stated otherwise.
(1) Default voltage setting for M_Config3.
(2) Default voltage setting for M_Config0, M_Config1 and M_Config2.
(3) Filter coil dc maximum resistance can go up to 200 mΩ, but conversion efficiency will decrease.
(4) Up to 20-µF capacitance can be placed in parallel to the Filter capacitor (C_L) without compromising the stability, however specification values above may change.
(5) Efficiency will be lowered as headroom voltage (V_{IN} − V_{OUT}) decreases to a minimum of 600 mV, particularly at higher output settings.

3.3 DCDC3 DC-DC Converter

DCDC3 is a programmable, synchronous buck switch converter having internal switch MOSFETs. The external inductor and capacitor are optimized for 1.2-MHz operation. The processor can force it into a sleep mode that improves efficiency under light load conditions. Table 3−5 shows the default configuration of DCDC3 register bits for each system state. A soft start circuit limits properly the inrush current.

Table 3−5. DCDC3 DC-DC Converter Electrical Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage (V_{IN})			2.8	V_{IN}	4.5	V
Output voltage	On mode: DCDC3_MODE[2:0] = 011, V_{OUT}+0.6V < V_{IN} < 4.5 V, 0 mA < I_O < 400 mA or Sleep mode: DCDC3_MODE[2:0] = 001, V_{OUT}+0.6 V < V_{IN} < 4.5 V, See Output current for I_{MAX} ratings	DCDC3_VOLT[2:0] = 000		1.5		V
		DCDC3_VOLT[2:0] = 001		1.8		
		DCDC3_VOLT[2:0] = 010		2.0		
		DCDC3_VOLT[2:0] = 011		2.2		
		DCDC3_VOLT[2:0] = 100		2.4		
		DCDC3_VOLT[2:0] = 101		2.8		
		DCDC3_VOLT[2:0] = 110		3.0		
		DCDC3_VOLT[2:0] = 111		3.2		
Output voltage accuracy	Inc. ripple, dc and transient line and load regulations, For maximum slew rate of 40 mA/µs at the output		−5		5	%
Output voltage accuracy	Inc. ripple, dc line and load regulations (without transient regulation)			3		%
Ground current (I_Q)	Off mode (at 85°C): DCDC3_MODE[2:0] = 000				1	µA
	Sleep mode: DCDC3_MODE[2:0] = 001, I_O = 0 mA max, 1.2 MHz				40	
	On mode: DCDC3_MODE[2:0] = 011, I_O = 0 mA max, 1.2 MHz				120	
Output current (I_{MAX}), Sleep mode	V_{OUT} = 1.5 to 1.8 V				10	mA
	V_{OUT} = 2.0 to 2.8 V				5	
	V_{OUT} = 3.0 V				2	
	V_{OUT} = 3.2 V				1	
Output current (I_{MAX}), On mode					400	mA
Short circuit current (I_{OS})	V_{IN} = V_{MAX}		700		Survival guaranteed	mA
Filter capacitor (C_L)	X5R or X7R		11	22	33(2)	µF
ESR of capacitor (R_{ESR})	f = 1.2 MHz		2		50	mΩ
Filter coil Inductance			3.29	4.70	6.11	µH

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Table 3−5. DCDC3 DC-DC Converter Electrical Characteristics (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter coil dc maximum resistance				125(1)	mΩ
Coil saturation current	Based on 30% inductance reduction from typical value	700			mA
Soft start current			190		mA
Load regulation	$0 < I_O < I_{MAX}$, V_{OUT} = 3.0 V		60		mV
Line regulation	V_{OUT} = 3.0 V		25		mV
Transient load regulation	I_O = 0 to I_{MAX}, V_{OUT} = 3.0 V, Max slew = 40 mA/µs		12		mV
Transient line regulation	300 mVpp ac square wave, with 10-µs rise/fall times, V_{OUT} = 3.0 V		5		mV
$t_{RECOVERY}$ (sleep to on or on to sleep mode)	In Sleep I_O = 5 mA, V_{IN} = V_{BAT} =2.8V In On I_O = 100 mA, V_{IN} = V_{BAT} =2.8V		30	50	µs
t_{ON}, Off to On	I_O = 0, C_L = 22 µF (within 5% of V_{OUT})		450	600	µs
t_{OFF}	V_{OUT} < 0.5 V			10	ms
Output shunt (pulldown) resistance	I_O = 1 µA		70		Ω
Overshoot	Off to On, I_O = 0			3	%
Conversion efficiency, On mode	I_O = 10 mA, V_{OUT} = 3.0 V		80		%
	I_O = 100 mA, V_{OUT} = 3.0 V		90		
	I_O = 400 mA, V_{OUT} = 3.0 V		90		
Conversion efficiency, Sleep mode	I_O = 10 mA, V_{OUT} = 1.8 V		85		%
	I_O = 5 mA, V_{OUT} = 3.0 V		43(3)		
Switching frequency			1200		kHz

All specifications are for default values only (in **bold**), unless stated otherwise.
(1) Filter coil dc max resistance can go up to 200 mΩ, but conversion efficiency will decrease.
(2) Up to 20-µF capacitance can be placed in parallel to the Filter capacitor (C_L) without compromising the stability, however specification values above may change.
(3) Efficiency will be lowered as headroom voltage (V_{IN} − V_{OUT}) decreases to a minimum of 600 mV, particularly at higher output settings.

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4 Low-Dropout Regulators (LDOR)

TWL92230 contains seven LDO regulators:

- LDO1 (VIO) − 200-mA LDO regulator (V_{OUT} = 1.50 V, 1.80 V, 2.50 V, or 2.80 V). It typically powers the processor I/O.
- LDO2 (VMEM) − 200-mA LDO regulator (V_{OUT} = 1.50 V, 1.80 V, 1.90 V, or 2.50 V). It typically powers memory.
- LDO3 (VMMC) − 200-mA LDO regulator (V_{OUT} = 1.85 V, 2.80 V, 3.00 V, or 3.10 V). It typically powers a Memory Card slot. MMC/SD Slot 1 (high-current level compliant with MMC/SD and SDIO 1.0).
- LDO4 (VPLL) − 10-mA, high-PSRR, low-noise LDO regulator (1.30 V). It typically powers the processor PLL.
- LDO5 (VAUX) − 200-mA LDO regulator (V_{OUT} = 1.50 V, 1.80 V, 2.50 V, or 2.80 V). It typically powers an extra device (flash memory, SDRAM, etc.).
- LDO6 (VDIG) − 5mA LDO regulator (1.80 V), used as the internal digital power supply. This LDO is not to be loaded externally.
- LDO7 (VADAC) − 2-mA, high-PSRR, low-noise LDO regulator (1.80 V). It typically powers the OMAP TV-out DAC.

All LDOs (except VDIG and VADAC) have three operating modes: Off, Sleep, and On. During the Off mode, the LDO is disabled, its quiescent current is minimum (<1 μA), and its output is grounded through a shunt pulldown resistor. Sleep mode is selected for light load operation, and a small PMOS pass device is used. In this mode, the LDO active circuits are consuming a small quiescent current, sufficient to meet specifications. On mode selects the normal operation requiring more quiescent current than Sleep mode. During the On mode, the LDO can meet all specifications at maximum output current.

The LDOs are designed for three modes of operation (except VDIG LDO).

Table 4−1. LDO Modes of Operation

MODE	XXX_MODE[1:0]	V_{OUT} (NOMINAL)	I_{OUT} (MAX)
Off	00	0	0
Sleep	01	Per Setting	Design Rating
On	1x	Per Setting	Design Rating

Register LDO_CTRL2 contains pulldown resistor bypass bits for each LDOs. The block diagram of these LDO regulators connected to typical external components in a typical configuration is shown in Figure 4−1.

All LDO input voltage terminals are recommended to have a 1-μF capacitor (X5R or X7R).

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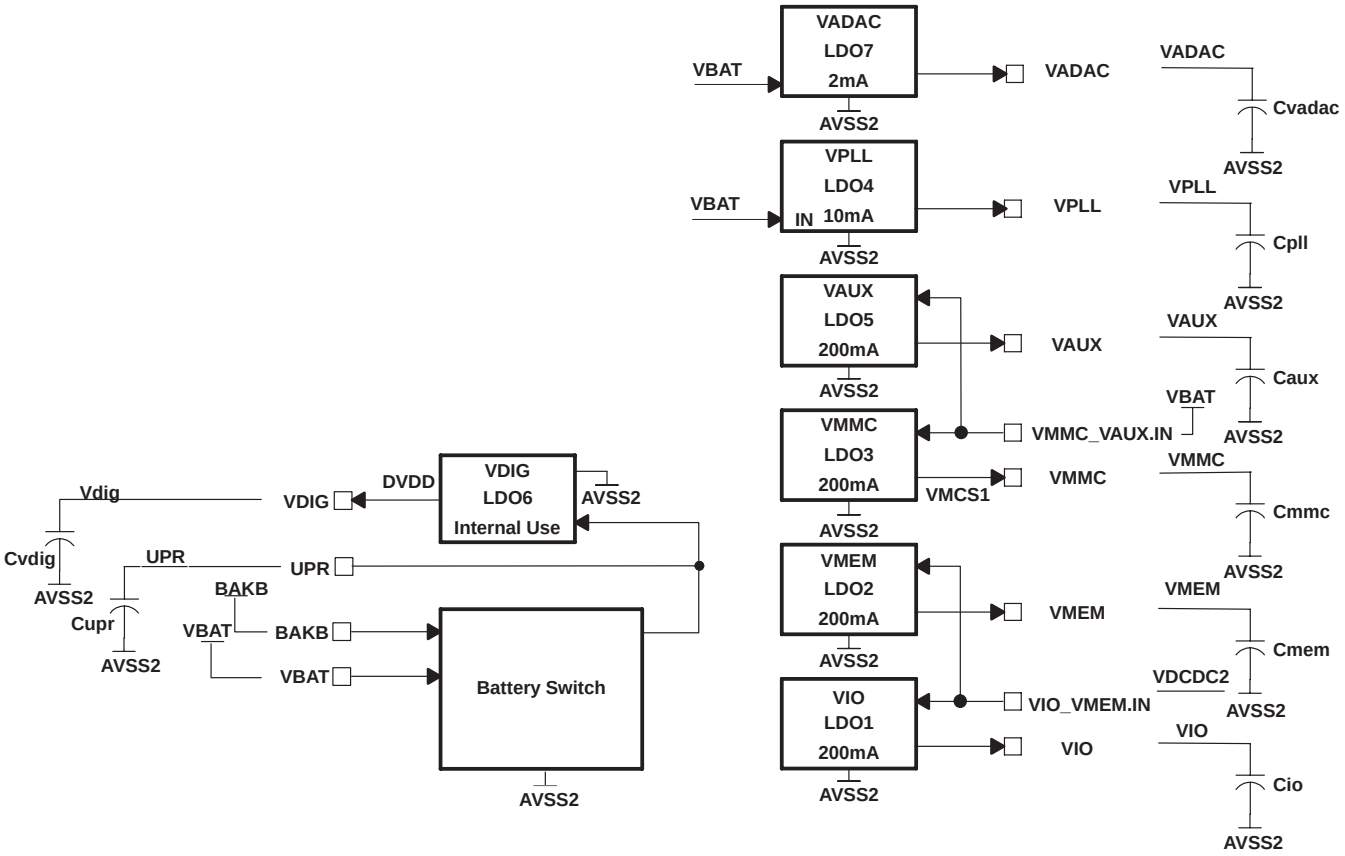


Figure 4−1. Typical Configuration of Low-Dropout Regulators and External Connections

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4.1 VIO LDO1 Regulator

VIO is a programmable low-dropout linear regulator, with four voltage settings. This LDO requires a 1-µF decoupling capacitor connected between the output terminal and GND. Table 4−2 shows the default configuration for each system state. The configuration can be changed by the processor by overwriting the register value.

The V_{IN} supply can be connected to a separate supply other than VBAT, but its voltage should not exceed VBAT.

Table 4−2. VIO LDO Regulator Electrical Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage (V_{IN})	$V_{IN} \le$ VBAT		2.0	V_{IN}	4.5	V
Output voltage (V_{OUT})	V_{OUT}+0.3 V < V_{IN} < 4.5 V, 0 mA < I_O < 200 mA, On: VIO_MODE[1:0] = 1x	VIO_VOLT[1:0] = 00		1.50		V
		VIO_VOLT [1:0] = 01		1.80		
		VIO_VOLT [1:0] = 10		2.50		
		VIO_VOLT [1:0] = 11		2.80		
Output voltage accuracy	Inc. dc load and line regulations (no transient regulation)		−3		+3	%
Ground current (I_Q)	Off: VIO_MODE[1:0] = 00				1	µA
	Sleep: VIO_MODE[1:0] = 01, I_O = 0 mA				15	
	Sleep: VIO_MODE[1:0] = 01, I_O = 5 mA				60	
	On: VIO_MODE[1:0] = 1x, I_O = 0 mA				50	
	On: VIO_MODE[1:0] = 1x, I_O = 100 mA				650	
Output current (I), Sleep mode					5	mA
Output current (I_{MAX}), On mode					200	mA
Short circuit current (I_{OS})	V_{OUT} = GND, On mode		400		700	mA
Filter capacitor (C_L)	X5R or X7R		0.7	1	3.3(2)	µF
ESR of capacitor (R_{ESR})	f = 100 kHz		10		100(1)	mΩ
Load regulation	0 < I_O < I_{MAX}			30		mV
Line regulation	(V_{OUT} + 0.3 V) < V_{IN} < 4.5 V, $V_{IN(MIN)}$ = 2 V, I_O = I_{MAX}				10	mV
Dropout voltage (V_{DROP})	I_O = I_{MAX}				300	mV
Transient load regulation	10% to 90% I_{MAX} in 1 µs, 90% to 10% I_{MAX} in 1 µs		−50		50	mV
Transient line regulation	300-mVpp ac square wave, with 10-µs rise/fall times			10		mV
t_{ON}	I_O = 0, C_L = 1 µF, within 10% of V_{OUT}, On mode				200	µs
$t_{RECOVERY}$ (sleep to on or on to sleep mode)	I_O = 5mA during recovery time				100	µs
t_{OFF}	V_{OUT} < 0.5 V				1(3)	ms
Overshoot	Off to On, I_O = 0				3	%
PSRR, f = 1.2 MHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			36		dB
PSRR, f = 20 Hz to 20 kHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			51		dB
Output shunt (pulldown) resistance	I_O = 1 µA			500		Ω

All specifications are for default values only (in **bold**), unless stated otherwise.

(1) This LDO is stable with up to 500 mΩ, however, specification values above may change.

(2) Up to 6.7-µF capacitance can be placed in parallel to the Filter capacitor (C_L) without compromising the stability, however specification values above may change.

(3) The MAX t_{OFF} delay timing is measured with a typical value of 1-µF filter capacitor (C_L). Delay is higher if the total capacitance exceeds the typical value.

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4.2 VMEM LDO2 Regulator

VMEM is a programmable low-dropout linear regulator, with four voltage settings. This LDO requires a 1-µF decoupling capacitor connected between the output terminal and GND. Table 4−3 shows the default configuration for each system state. The configuration can be changed by the processor by overwriting the register value.

The V_{IN} supply can be connected to a separate supply other than VBAT, but its voltage should not exceed VBAT.

Table 4−3. VMEM LDO2 Regulator Electrical Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage (V_{IN})	$V_{IN} \le$ VBAT		2.0	V_{IN}	4.5	V
Output voltage (V_{OUT})	V_{OUT}+0.3 V < V_{IN} < 4.5 V 0 mA < I_O < 200 mA On: VMEM_MODE[1:0] = 1x	VMEM_VOLT [1:0] = 00		1.50		V
		VMEM_VOLT [1:0] = 01		**1.80**		
		VMEM_VOLT [1:0] = 10		1.90		
		VMEM_VOLT [1:0] = 11		2.50		
Output voltage accuracy	Inc. dc load and line regulations (no transient regulation)		−3		+3	%
Ground current (I_Q)	Off: VMEM_MODE[1:0] = 00				1	µA
	Sleep: VMEM_MODE[1:0] = 01, I_O = 0 mA				15	
	Sleep: VMEM_MODE[1:0] = 01, I_O = 5 mA				60	
	On: VMEM_MODE[1:0] = 1x, I_O = 0 mA				50	
	On: VMEM_MODE[1:0] = 1x, I_O = 100 mA				650	
Output current (I_{MAX}), Sleep mode					5	mA
Output current (I_{MAX}), On mode					200	mA
Short circuit current (I_{OS})	V_{OUT} = GND, On mode		400		700	mA
Filter capacitor (C_L)	X5R or X7R		0.7	1	3.3(2)	µF
ESR of capacitor (R_{ESR})	f = 100 kHz		10		100(1)	mΩ
Load regulation	0 < I_O < I_{MAX}			30		mV
Line regulation	(V_{OUT} + 0.3 V) < V_{IN} < 4.5 V, $V_{IN(MIN)}$ = 2 V, I_O = I_{MAX}				10	mV
Dropout voltage (V_{DROP})	I_O = I_{MAX}				300	mV
Transient load regulation	10% to 90% I_{MAX} in 1 µs 90% to 10% I_{MAX} in 1 µs		−50		50	mV
Transient line regulation	300-mVpp ac square wave, with 10-µs rise/fall times			10		mV
t_{ON}	I_O = 0, C_L = 1 µF, within 10% of V_{OUT}, On mode				200	µs
$t_{RECOVERY}$ (sleep to on or on to sleep mode)	I_O = 5mA during recovery time				100	µs
t_{OFF}	V_{OUT} < 0.5 V				1(3)	ms
Overshoot	Off to On, I_O = 0				3	%
PSRR, f = 1.2 MHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			36		dB
PSRR, f = 20 Hz to 20 kHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			51		dB
Output shunt (pulldown) resistance	I_O = 1 µA			500		Ω

All specifications are for default values only (in **bold**), unless stated otherwise.

(1) This LDO is stable with up to 500 mΩ, however specification values above may change.

(2) Up to 6.7-µF capacitance can be placed in parallel to the Filter capacitor (C_L) without compromising the stability, however specification values above may change.

(3) The MAX t_{OFF} delay timing is measured with a typical value of 1-µF filter capacitor (C_L). Delay is higher if the total capacitance exceeds the typical value.

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4.3 VMMC LDO3 Regulator

VMMC is a programmable low-dropout linear regulator, with four voltage settings. This LDO requires a 1-µF decoupling capacitor connected between the output terminal and GND. Table 4−4 shows the default configuration for each system state. The configuration can be changed by the processor by overwriting the register value.
The V_{IN} supply can be connected to a separate supply other than VBAT, but it's voltage should not exceed VBAT.

Table 4−4. VMMC LDO3 Regulator Electrical Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage (V_{IN})	$V_{IN} \le$ VBAT		2.0	V_{IN}	4.5	V
Output voltage (V_{OUT})	V_{OUT}+0.2 V < V_{IN} < 4.5 V 0 mA < I_O < 200 mA On: VMMC_MODE[1:0] = 1x	VMMC_VOLT [1:0] = 00		1.85(3)		V
		VMMC_VOLT [1:0] = 01		2.80		
		VMMC_VOLT [1:0] = 10		**3.00**		
		VMMC_VOLT [1:0] = 11		3.10		
Output voltage accuracy	Inc. dc load and line regulations (no transient regulation)		−3		3	%
Ground current (I_Q)	Off: VMMC_MODE[1:0] = 00				1	µA
	Sleep: VMMC_MODE [1:0] = 01, I_O = 0 mA				15	
	Sleep: VMMC_MODE[1:0] = 01, I_O = 5 mA				60	
	On: VMMC_MODE [1:0] = 1x, I_O = 0 mA				50	
	On: VMMC_MODE [1:0] = 1x, I_O = 100 mA				650	
Output current (I_{MAX}), Sleep mode					5	mA
Output current (I_{MAX}), On mode	V_{OUT} = 1.85 V				180	mA
	V_{OUT} = 2.80 V, 3.00 V, 3.10 V				200	
Short circuit current (I_{OS})	V_{OUT} = GND, On mode		400		700	mA
Filter capacitor (C_L)	X5R or X7R		0.7	1	3.3(2)	µF
ESR of capacitor (R_{ESR})	f = 100 kHz		10		100(1)	mΩ
Load regulation	0 < I_O < I_{MAX}			30		mV
Line regulation	(V_{OUT} + 0.2 V) < V_{IN} < 4.5 V, $V_{IN(MIN)}$ = 2 V, I_O = I_{MAX}				10	mV
Dropout voltage (V_{DROP})	I_O = I_{MAX}				200(3)	mV
Transient load regulation	10% to 90% I_{MAX} in 1 µs, 90% to 10% I_{MAX} in 1 µs		−50		50	mV
Transient line regulation	300-mVpp ac square wave, with 10-µs rise/fall times			10		mV
t_{ON}	I_O = 0, C_L = 1 µF, within 10% of V_{OUT}, On mode				200	µs
$t_{RECOVERY}$ (Sleep to On mode or On to Sleep mode)	I_O = 5mA during recovery time				100	µs
t_{OFF}	V_{OUT} < 0.5 V				1(4)	ms
Overshoot	Off to On, I_O = 0				3	%
PSRR, f = 1.2 MHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			36		dB
PSRR, f = 20 Hz to 20 kHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			51		dB
Output shunt (pulldown) resistance	I_O = 1 µA			500		Ω

All specifications are for default values only (in **bold**), unless stated otherwise.
(1) This LDO is stable with up to 500 mΩ, however specification values above may change.
(2) Up to 6.7-µF capacitance can be placed in parallel to the Filter capacitor (C_L) without compromising the stability, however specification values above may change.
(3) Maximum dropout voltage (V_{DROP}) is 300 mV for V_{OUT} = 1.85 V.
(4) The MAX t_{OFF} delay timing is measured with a typical value of 1-µF filter capacitor (C_L). Delay is higher if the total capacitance exceeds the typical value.

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4.4 VAUX LDO5 Regulator

VAUX is a programmable low-dropout linear regulator, with four voltage settings. This LDO requires a 1-µF decoupling capacitor connected between the output terminal and GND. Table 4−5 shows the default configuration for each system state. The configuration can be changed by the processor by overwriting the register value.

The V_{IN} supply can be connected to a separate supply other than VBAT, but its voltage should not exceed Vbat.

Table 4−5. VAUX LDO5 Regulator Electrical Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage (V_{IN})	VIN <= VBAT		2.0	V_{IN}	4.5	V
Output voltage (V_{OUT})	V_{OUT}+0.3 V < V_{IN} < 4.5 V 0 mA < I_O < 200 mA On: VAUX_MODE[1:0] = 1x	VAUX_VOLT[1:0] = 00		1.50		V
		VAUX_VOLT[1:0] = 01		**1.80**		
		VAUX_VOLT[1:0] = 10		2.50		
		VAUX_VOLT[1:0] = 11		2.80		
Output voltage accuracy	Inc. dc load and line regulations (no transient regulation)		−3		3	%
Ground current (I_Q)	Off: VAUX_MODE[1:0] = 00				1	µA
	Sleep: VAUX_MODE[1:0] = 01, I_O = 0 mA				15	
	Sleep: VAUX_MODE[1:0] = 01, I_O = 5 mA				60	
	On: VAUX_MODE[1:0] = 1x, I_O = 0 mA				50	
	On: VAUX_MODE[1:0] = 1x, I_O = 100 mA				650	
Output current (I_{MAX}), sleep mode					5	mA
Output current (I_{MAX}), On mode					200	mA
Short circuit current (I_{OS})	V_{OUT} = GND, On mode		400		700	mA
Filter capacitor (C_L)	X5R or X7R		0.7	1	3.3(2)	µF
ESR of capacitor (R_{ESR})	f = 100 kHz		10		100(1)	mΩ
Load regulation	0 < I_O < I_{MAX}			30		mV
Line regulation	(V_{OUT} + 0.3 V) < V_{IN} < 4.5 V, $V_{IN(MIN)}$ = 2 V, I_O = I_{MAX}				10	mV
Dropout voltage (V_{DROP})	I_O = I_{MAX}				300	mV
Transient load regulation	10% to 90% I_{MAX} in 1 µs 90% to 10% I_{MAX} in 1 µs		−50		50	mV
Transient line regulation	300-mVpp ac square wave, with 10-µs rise/fall times			10		mV
t_{ON}	I_O = 0, C_L = 1 µF, within 10% of V_{OUT}, On mode				200	µs
$t_{RECOVERY}$ (sleep to on or on to sleep mode)	I_O = 5 mA during recovery time				100	µs
t_{OFF}	V_{OUT} < 0.5 V				1(3)	ms
Overshoot	Off to On, I_O = 0				3	%
PSRR, f = 1.2 MHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			36		dB
PSRR, f = 20 Hz to 20 kHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			51		dB
Output shunt (pulldown) resistance	I_O = 1 µA			500		Ω

All specifications are for default values only (in **bold**), unless stated otherwise.

(1) This LDO is stable with up to 500 mΩ, however specification values above may change.

(2) Up to 6.7-µF capacitance can be placed in parallel to the Filter capacitor (C_L) without compromising the stability, however, specification values above may change.

(3) The MAX t_{OFF} delay timing is measured with a typical value of 1-µF filter capacitor (C_L). Delay is higher if the total capacitance exceeds the typical value.

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4.5 VPLL LDO4 Regulator

VPLL is a programmable low-dropout linear regulator, with four voltage settings. This high-PSRR low-noise LDO requires a 1-µF decoupling capacitor connected between the output terminal and GND. Table 4−6 shows the default configuration for each system state. The configuration can be changed by the processor by overwriting the register value.

Table 4−6. VPLL LDO4 Regulator Electrical Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage (V_{IN})			2.8	VBAT	4.5	V
Output voltage (V_{OUT})	2.8 V < V_{IN} < 4.5 V 0 mA < I_O < 10 mA On: VPLL_MODE[1:0] = 1x	VPLL_VOLT[1:0] = 00		1.05		V
		VPLL_VOLT[1:0] = 01		1.20		
		VPLL_VOLT[1:0] = 10		**1.30**		
		VPLL_VOLT[1:0] = 11		1.40		
Output voltage accuracy	Inc. dc load and line regulations (no transient regulation)		−3		+3	%
Ground current (I_Q)	Off: VPLL_MODE[1:0] = 00				1	µA
	Sleep: VPLL_MODE[1:0] = 01, I_O = 0 mA				15	
	Sleep: VPLL_MODE[1:0] = 01, I_O = 600 µA				20	
	On: VPLL_MODE[1:0] = 1x, I_O = 0 mA				40	
	On: VPLL_MODE[1:0] = 1x, I_O = 5 mA				200	
Output current (I_{MAX}), Sleep mode					600	µA
Output current (I_{MAX}), On mode					10	mA
Short circuit current (I_{OS})	V_{OUT} = GND, On mode		100		200	mA
Filter capacitor (C_L)	X5R or X7R		0.7	1	3.3	µF
ESR of capacitor (R_{ESR})	f = 100 kHz		10		100(1)	mΩ
Load regulation	0 < I_O < I_{MAX}			1.5		mV
Line regulation	2.8 V < V_{IN} < 4.5 V, I_O = I_{MAX}				10	mV
Transient load regulation	10% to 90% I_{MAX} in 1 µs 90% to 10% I_{MAX} in 1 µs		−30		30	mV
Transient line regulation	300-mVpp ac square wave, with 10-µs rise/fall times			5		mV
t_{ON}	I_O = 0, C_L = 1 µF, within 10% of V_{OUT}, On mode				250	µs
$t_{RECOVERY}$ (Sleep to On mode or On to Sleep mode)	I_O = 5mA during recovery time				100	µs
t_{OFF}	V_{OUT} < 0.5 V				1(2)	ms
Overshoot	Off to On, I_O = 0				3	%
PSRR f = 20 Hz to 20 kHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			64		dB
PSRR f = 1.2 MHz	I_O = I_{MAX}/2, On mode, V_{IN} = VBAT = 2.8 V			60		dB
Output shunt (pulldown) resistance	I_O = 1 µA			500		Ω

All specifications are for default values only (in **bold**), unless stated otherwise.
(1) This LDO is stable with up to 500 mΩ, however specification values above may change.
(2) The MAX t_{OFF} delay timing is measured with a typical value of 1-µF filter capacitor (C_L). Delay is higher if the total capacitance exceeds the typical value.

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4.6 VDIG LDO6 Regulator

VDIG is a fixed low-dropout linear regulator that is parametric compliant for VBAT down to 2.4 V. This LDO requires a 1-µF decoupling capacitor connected between the output terminal and GND. This LDO can be used to power all internal digital circuits, and contains a low-current bandgap reference (it does not use the main bandgap present in the REFSYS block). Table 4−7 shows the default configuration for each system state.

Table 4−7. VDIG LDO6 Regulator Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (V_{IN})		2.4	VBAT	4.5	V
Output voltage (V_{OUT})	2.4 V < V_{IN} < 4.5 V, 0 mA < I_O < 5 mA		1.8		V
Output voltage accuracy	Inc. dc load and line regulations (no transient regulation) Includes internal VDIG bandgap	−4		4	%
Ground current (I_Q)	I_O = 0 mA		5	10	µA
Output current (I_{MAX})				5	mA
Short circuit current (I_{OS})	V_{OUT} = GND			300	mA
Filter capacitor (C_L)	X5R or X7R	0.7	1	3.3	µF
ESR of capacitor (R_{ESR})	f = 100 kHz			100(1)	mΩ
Load regulation	0 < I_O < I_{MAX}		0.5		mV
Line regulation	2.4 < V_{IN} < 4.5 V, I_O = I_{MAX}			10	mV
Transient load regulation	10% to 90% I_{MAX} in 1 µs 90% to 10% I_{MAX} in 1 µs	−50		50	mV
t_{ON}	I_O = 0, C_L = 1 µF, within 10% of V_{OUT}		0.3	1	ms
PSRR	f = 20 Hz to 20 kHz, I_O = I_{MAX}/2		40		dB

All specifications are for default values only (in **bold**), unless stated otherwise.
(1) This LDO is stable with up to 500 mΩ, however specification values above may change.

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4.7 VADAC LDO7 Regulator

VADAC is a low-dropout linear regulator with a 1.8-V voltage output. This high-PSRR low-noise LDO requires a 1-µF decoupling capacitor connected between the output terminal and GND. Table 4−8 shows the default configuration for each system state. The configuration can be changed by the processor by overwriting the register value.

Table 4−8. VADAC LDO7 Regulator Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (V_{IN})		2.8	VBAT	4.5	V
Output voltage (V_{OUT})	2.8 V < V_{IN} < 4.5 V 0 mA < I_O < 2 mA On: VADAC_EN = 1		1.8		V
Output voltage accuracy	Inc. dc load and line regulations (no transient regulation)	−3		+3	%
Ground current (I_Q)	Off: VADAC_EN = 0			1	µA
	On: VADAC_EN = 1, I_O = 0 mA			40	
	On: VADAC_EN = 1, I_O = 2 mA			200	
Output current (I_{MAX}), On mode				2	mA
Short circuit current (I_{OS})	V_{OUT} = GND, On mode	100		200	mA
Filter capacitor (C_L)	X5R or X7R	0.7	1	3.3	µF
ESR of capacitor (R_{ESR})	f = 100 kHz			100(1)	mΩ
Load regulation	0 < I_O < I_{MAX}		0.5		mV
Line regulation	2.8 V < V_{IN} < 4.5 V, I_O = I_{MAX}			10	mV
Transient load regulation	10% to 90% I_{MAX} in 1 µs 90% to 10% I_{MAX} in 1 µs	−30		30	mV
Transient line regulation	300 mVpp ac square wave, with 10-µs rise/fall times		5		mV
t_{ON}	I_O = 0, C_L = 1 µF, within 10% of V_{OUT}, On mode			250	µs
t_{OFF}	V_{OUT} < 0.5 V			1(2)	ms
Overshoot	Off to On, I_O = 0			3	%
PSRR, f = 10 Hz to 100 kHz	I_O = I_{MAX}/2, On mode, VBAT = 2.8 V 300mVpp superimposed on V_{IN}	32(3)	50		dB
PSRR, f = 100 kHz to 6 MHz	I_O = I_{MAX}/2, On mode, VBAT = 2.8 V 300mVpp superimposed on V_{IN}	32(3)	50		dB
Output Noise Spectral Density	BW = 10 Hz to 100 kHz			20	$\frac{\mu V}{\sqrt{Hz}}$
	BW = 100 kHz to 1 MHz			2	
	BW = 1 MHz to 10 MHz			0.2	
Output shunt (pulldown) resistance	I_O = 1 µA		500		Ω

All specifications are for default values only (in **bold**), unless stated otherwise.
(1) This LDO is stable with up to 500 mΩ, however specification values above may change.
(2) The MAX t_{OFF} delay timing is measured with a typical value of 1-µF filter capacitor (C_L). Delay is higher if the total capacitance exceeds the typical value.
(3) PSRR minimum value is compliant with OMAP requirement.

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5 Reference System (REFSYS)

The REFS_BG500 block consists of a buffered Bandgap Reference. This block can be turned on or turned off by writing to the REF05_EN register bit. REFS_BG500 is off when REF05_EN = 0 (default condition).

The REFSYS block consists of a Bandgap Reference, Bias Current Generator, Thermal Shutdown and Hot Die Detectors.

5.1 Bandgap Reference

The bandgap voltage reference is filtered using an external 100-nF capacitor connected across the BG_CAP terminal and an analog ground (AVSS1). The VREF voltage is distributed and buffered inside the device. The bandgap voltage is trimmed during production test and the trimming value is stored in the EEPROM.

Table 5−1. Bandgap Reference Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Bandgap output voltage on BG_CAP	ACTIVE mode, after trimming		0.85		V
Bandgap accuracy	ACTIVE mode, after trimming	−1		+1	%
Bandgap startup	Settling at 1%			500	µs
Ground current (IQ)				50	µA
Filter capacitor (C_L)	X5R or X7R		100(1)	120	nF

(1) An alternative capacitor of 470 nF ± 30% can be substituted to reduce any potential overshoot at the startup. The maximum startup time will increase to 1700 µs.

5.2 TV-Out 0.5-V Reference (REFS_BG500)

This reference is filtered (RC filter) using an external 100-nF capacitor connected across the VREF05 terminal and an analog ground (AVSS1). This voltage is not used inside the device. This voltage does not need to be trimmed.

Table 5−2. TV-Out 0.5-V Reference Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output voltage on REFS_BG500			0.50		V
Accuracy		−2.5		+2.5	%
Startup	Settling at 1%			500	µs
Internal Resistance (used for output RC filter)			100		Ω
Ground current (IQ)				15	µA
Output current (I_{MAX}), On mode				10	nA
PSRR, f = 10 Hz to 1 MHz	$I_O = I_{MAX}/2$, On mode, VBAT = 2.8 V		60		dB
PSRR, f = 10MHz	$I_O = I_{MAX}/2$, On mode, VBAT = 2.8 V		40		dB
Output Integrated Noise	BW = 10 Hz to 6 MHz			40	µVrms
Filter capacitor (C_L)	X5R or X7R	70	100	130	nF

5.3 Bias Current Generator

This circuit provides both source and sink 1-µA bias currents for all other analog circuits.

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5.4 Thermal Shutdown Detector

This circuit monitors the junction temperature of the TWL92230. Thermal shutdown circuitry is enabled when a valid voltage is applied to VBAT (that is, the voltage on VBAT is greater than $V_{UVLO-TH}$). If the junction reaches a temperature at which damage can occur, all regulators are disabled by hardware and thermal shutdown information is written to the interrupt register (INT_STATUS1). Operation is restored (all registers are reset and the TWL92230 restarts with default values) after the junction temperature falls 35°C and an appropriate power-on sequence takes place, with the application processor been notified of this occurrence by the interrupt signal (INT). When the TWL92230 is in test mode, a thermal shutdown bypass mode is available so this circuit is disabled to allow an accelerated life test. An interrupt mask bit is available for the thermal shutdown. The entire path is guaranteed to be fully functional when the VDIG LDO regulator is parametric compliant.

Table 5−3. Thermal Shutdown Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
JT_{TS}	Thermal shutdown − junction temperature	T_J increasing	145	165	185	°C
ΔJT_{TSH}	Thermal shutdown − hysteresis			50		°C

5.5 Hot Die Detector

This circuit also monitors the junction temperature of the TWL92230, but it does not shutdown the TWL92230. This detector provides an early warning to the application processor to avoid excessive power dissipation and therefore to avoid a thermal shutdown. The temperature of the hot die detector is set several degrees below the thermal shutdown threshold. If the junction temperature reaches the hot die junction temperature (THDTH), an interrupt (INT) is sent and this information is present in the interrupt register (INT_STATUS1). The application processor must take immediate action to reduce the amount of power drawn from the TWL92230. If corrective action is not taken and the die temperature continues to climb, the thermal shutdown may trigger a system reset to protect the device.

An over-temperature condition exists if this register bit is high. The hot die detector is always enabled, but an interrupt mask bit is available for it. The entire path is functional whenever the VDIG LDO regulator is operational.

Table 5−4. Hot Die Detector Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
JT_{HD}	Hot die junction temperature	T_J increasing	135	145	155	°C
ΔJT_{TS-HD}	Difference between thermal shutdown temperature threshold and hot die temperature threshold		10			°C
ΔJT_{HDH}	Hot die hysteresis			20		°C

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5.6 Hot Die and Thermal Shutdown Behavior

TWL92230 includes two thermal detection circuitries:

- Hot die
- Thermal shutdown

The temperature thresholds are implemented in the following manner:

Thermal shutdown recovery **<** Hot die recovery **<** Hot die detection **<** Thermal shutdown detection

The hot die detection and hot die recovery thresholds are between the thermal shutdown detection and the thermal shutdown recovery thresholds. This is to ensure that after a thermal shutdown, TWL92230 will recover at a temperature below the *thermal shutdown recovery* threshold.

When reaching the *hot die detection* level, TWL92230 will assert an interrupt to OMAP. OMAP through I2C will read the interrupt register and the *hot die detection* interrupt is detected by OMAP. As long as TWL92230 is in a *hot die detection* condition, TWL92230 will send an interrupt to OMAP.

To avoid this behavior, it is up to OMAP to mask the *hot die detection* interrupt and then enter in a “Clear hot die detection interrupt / Read the HOTDIE bit” mode. This is a polling mode to check whether or not TWL92230 is in a *hot die detection* condition. If after clearing the HOTDIE bit, OMAP reads back this bit at “1”, then it means that TWL92230 is still under a *hot die detection* condition.

When TWL92230 temperature has raised above the *hot die detection* threshold, then it asserts the HOTDIE bit. To exit from this *hot die detection* condition, TWL92230 temperature must decrease below the *hot die recovery* temperature.

Therefore, if after a *hot die detection* condition, the temperature continues to rise then TWL92230 temperature can reach the *thermal shutdown* threshold. When TWL92230 temperature reaches the *thermal shutdown* threshold, TWL92230 asserts the TSHUT bit and immediately shuts down.

As long as TWL92230 temperature remains above the *thermal shutdown recovery* threshold, TWL92230 remains turned off.

When TWL92230 temperature is back below the *thermal shutdown recovery* threshold, TWL92230 automatically initiates a startup sequence. After the startup sequence is complete, OMAP can read the interrupt register status and check the TSHUT bit.

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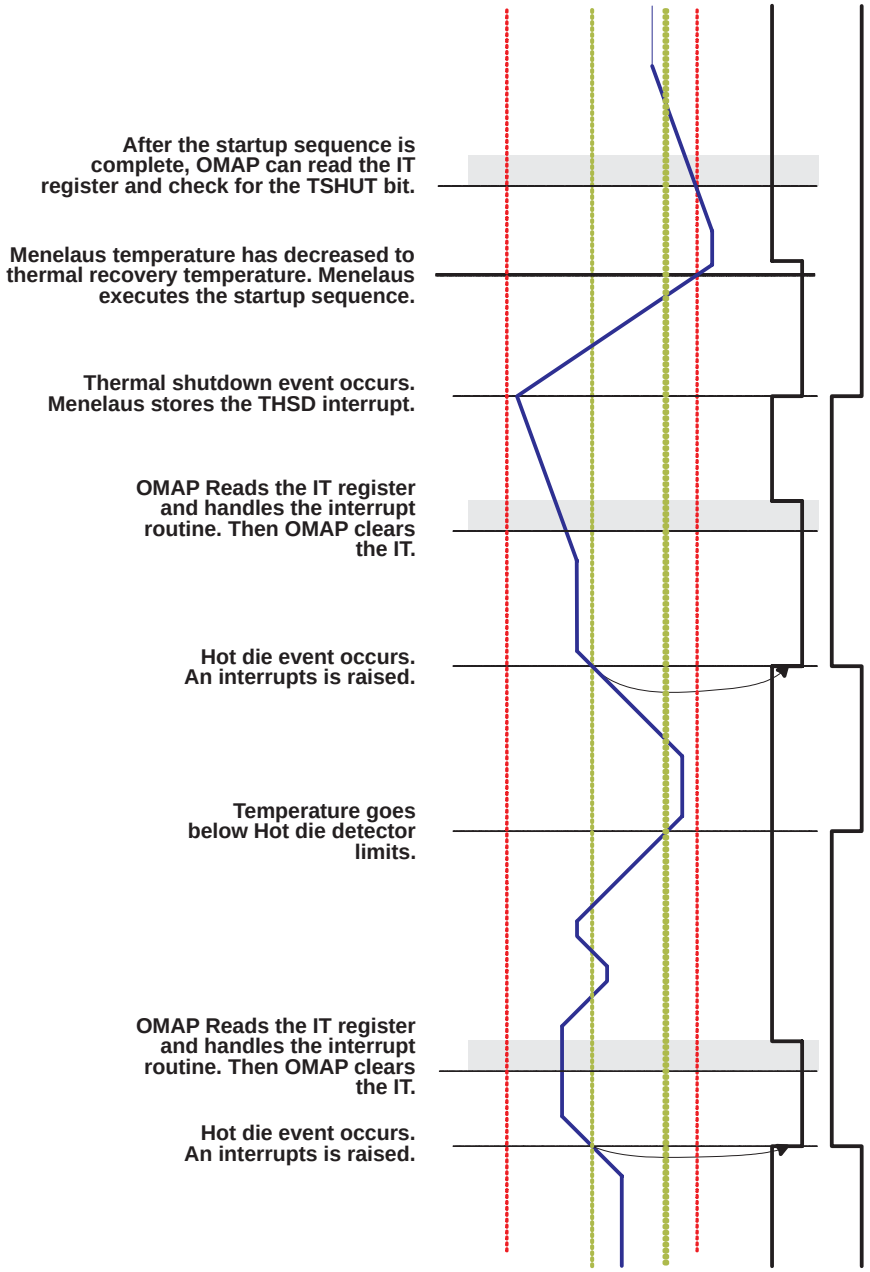


Figure 5−1. Hot Die and Thermal Shutdown Behavior

6 Clock Generator System (CLKGEN)

The CLKGEN block contains the 32-kHz oscillator, the 600-kHz oscillator, the 1.2-MHz Ramp Generator and the High-frequency clock slicer. The 600 kHz is used for debouncing and for the startup. The CLKGEN block diagram is shown below.

The internal 1.2-MHz oscillator generates the clock for the buck converters. The internal 600 kHz oscillator generates the clock for all digital circuitry. When the external 12 MHz, 13 MHz, or 19.2 MHz clock signal is present and when the HFCLK_SEL bits are properly configured, the oscillators lock onto this external clock in less than 1 600-kHz clock cycle. During operation the HFCLK signal may come and go without affecting the operation of the oscillators. The oscillators are activated or deactivated by internal signals when needed by internal blocks to complete a task.

The 600K_OUT clock is enabled when either 600K_REQ = 1 or 1P2M_REQ = 1. The 600K_OUT clock is synchronized to the 600K_IN clock if present (the 600K_IN clock does not need to be present for the 600-kHz oscillator to operate). The 1.2-MHz oscillator needs the 600K_OUT clock to operate properly. Therefore, it is not possible to enable the 1.2-MHz oscillator without enabling the 600-kHz oscillator as well.

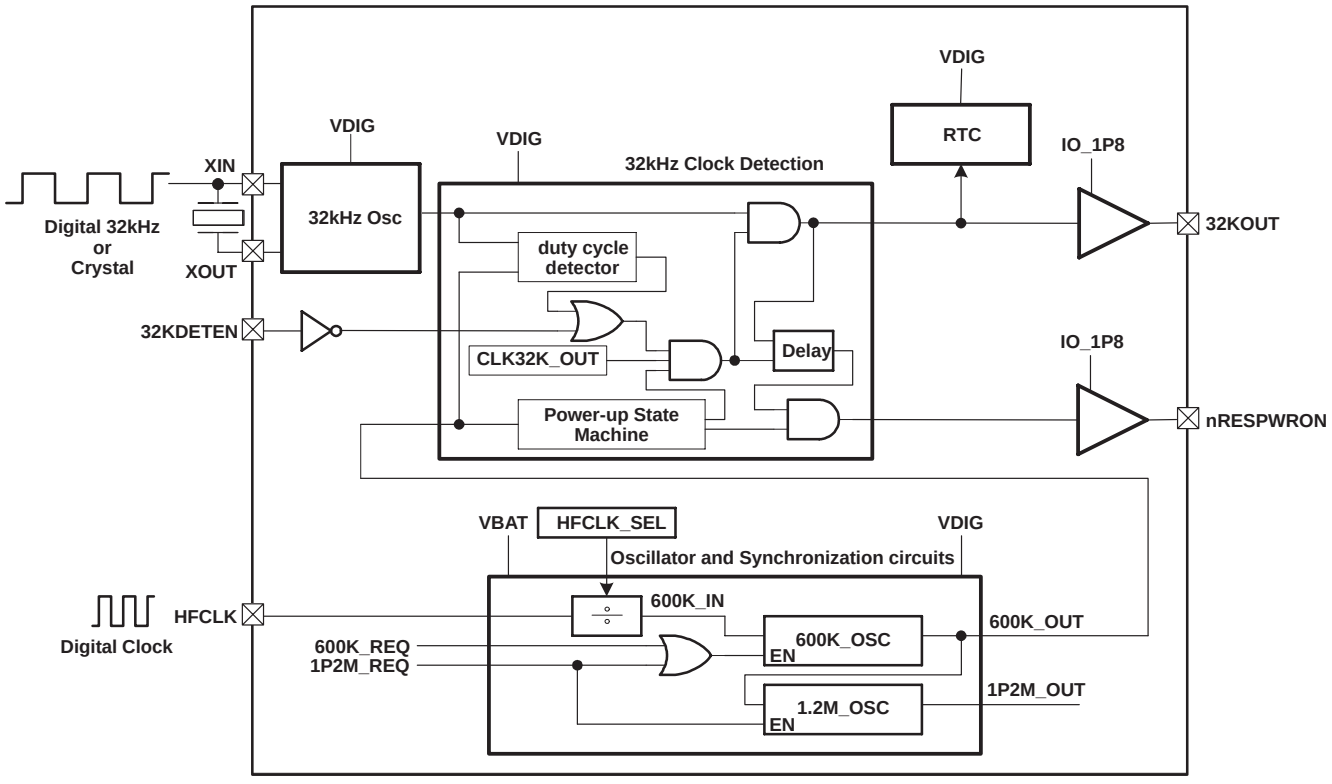


Figure 6−1. Clock Generator Block Diagram

A 32-kHz clock is required for the RTC functionality, however TWL92230 can still operate without it. A 32-kHz crystal oscillator can be connected to the TWL92230, or a digital 32-kHz clock should be applied to the XIN terminal.

The 32-kHz output is dedicated for the application processor for a safe power-on and power-off sequence.

The CLKGEN block contains an auto-detect feature that switches to the internal 1.2MHz clock oscillator, if no signal is present at the HFCLK terminal.

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6.1 32-kHz Oscillator

The TWL92230 includes a 32-kHz crystal oscillator circuit. A crystal can be connected across XIN and XOUT terminals, or an external 32-kHz digital clock can be directly applied to the XIN terminal (with the XOUT floating). This requires no configuration and the 32-kHz oscillator circuitry does not need to be disabled. The oscillator output is used within the TWL92230 for use by the real-time clock only. The 32-kHz crystal oscillator is powered by the VDIG LDO and has very low-power consumption. A digital 32-kHz clock output (32KOUT terminal) can be broadcasted externally to the application processor or to other devices.

6.2 32-kHz Integrity Detection

There is a 32-kHZ integrity-detection circuit enabled by an external pin (32KDETEN). When this pin is asserted LOW, the detector will be bypassed and the nRESPWRON will rise at the normal startup scheduled time. If 32KDETEN pin is tied to VDIG (HIGH prior to startup), the nRESPWRON will be held low during the startup sequence until valid 32K clock cycles (duty cycle of approximately 20%/80% (80%/20%) or better) are completed. The detector uses the internal 600K clock to detect the 32K clock; this is to insure the 32K clock is valid and available prior to nRESPWRON rise. See section 10.17 for additional implementation description.

Table 6−1. 32-kHz Oscillator Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating voltage	Oscillator and RTC block	1.7		2.4	V
Operating current	VDIG = 1.8 V, T = 25°C			3	µA
Oscillator startup time	Crystal on XTAL pins, step VBAT 0 V to 3.2 V, T = −30°C to +85°C		0.8	4	s
External capacitor on XIN or XOUT pin				30	pF
XIN duty cycle DIGITAL	External signal source	20		80	%
Leakage: XIN to GND	External leakage from PCB and load capacitors, after power-up.			10	nA
Leakage: XIN to XOUT	External leakage from PCB and load capacitors, after power-up.			10	nA
External series resistance on XIN	Needed for current limiting if an external clock is applied before TWL92230 power-up.		100		kΩ
Crystal	Micro Crystal MS2V-TS				
Crystal frequency tolerances		−30		+30	ppm
Total frequency stability	Combination of crystal, manufacturing, and temperature	−100		+100	ppm

Table 6−2 contains the relevant electrical specifications for the crystal used for this oscillator.

Table 6−2. Crystal Electrical Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Frequency		32768		Hz
Series resistance	20		90	kΩ
Motional capacitance	1		2.7	pF
Shunt capacitance	0.6		1.8	pF
Quality factor		50000		
Isolation resistance	100			mΩ
Drive level			1	µW

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6.3 RAMP (1.2-MHz Internal Oscillator)

The RC oscillator generates the clock for the digital logic. It is enabled by default at startup and goes in standby mode when the TWL92230 returns to the M_WaitOn state. The RC oscillator can be stopped when a high-frequency clock is available.

The 600-kHz oscillator and the 1.2-MHz ramp generator are powered by VBAT.

Table 6−3. 1.2-MHz Internal Oscillator Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating voltage	V_{IN} = VBAT	2.4	3.6	4.5	V
I_{OSC}	Current consumption	Both 1.2 MHz and 600 kHz are ON			40	µA
f_{OSC}	Internal frequency		1.08	1.2	1.32	MHz
t_{R_OSC} t_{F_OSC}	Rise and fall time			8		ns
$t_{OSC-START}$	Start-up time	After bandgap is stable			50	µs
$t_{OSC-LOCK}$	Lock-in time	In ON or Standby mode			2	µs

Table 6−4. 600-kHz Internal Oscillator Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating voltage	V_{IN} = VBAT	2.4	3.6	4.5	V
I_{OSC}	Current consumption	Only 600 kHz is ON			35	µA
f_{OSC}	Internal frequency		540	600	660	kHz
t_{R_OSC} t_{F_OSC}	Rise and fall time			8		ns
$t_{OSC-START}$	Start-up time	After Bandgap is stable			50	µs
$t_{OSC-LOCK}$	Lock-in time	In ON or Standby mode			2	µs

6.4 High Frequency Clock (HFCLK)

When a digital high frequency clock is available in the system, it can be used by the TWL92230 to synchronize the 1.2-MHz and 600-kHz oscillators for the dc-dc converters and the logic. This can reduce noise disturbance in the system and reduces the RC oscillator power consumption when the HFCLK_SEL bits are properly configured (see Table 6−5 and Figure 5−1).

Table 6−5. HFCLK Slicer Modes of Operation

6.5 Clock Arbitration

By default, the clock used for the dc-dc converters and the logic in TWL92230 is the RC oscillator.

The following sequence must be followed to use the HFCLK:

1. OMAP sets up, via I^2C, the HFCLK_SEL bits to select the clock frequency on the HFCLK terminal.
2. The RC oscillators goes automatically to standby mode when the HFCLK is present, and goes automatically to on-mode when the HFCLK is removed.

The HFCLK frequency must not be changed after the high-frequency selection is made, or the oscillator may lock in at an undetermined frequency.

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7 Backup Battery Switch and Monitoring System (BBSMS)

The backup battery switch (BBS) generates at its output an uninterrupted power rail (UPR) to supply the minimum necessary circuitry of the power-control functions continuously, either from the main battery or from the backup battery. This UPR is connected to an output terminal (UPR) for decoupling purposes. The UPR switch is usually connected to VBAT (default condition), but it can automatically change its connection to the Backup Battery BAKB when UVLO = 1.

7.1 Configuration With a Backup Battery

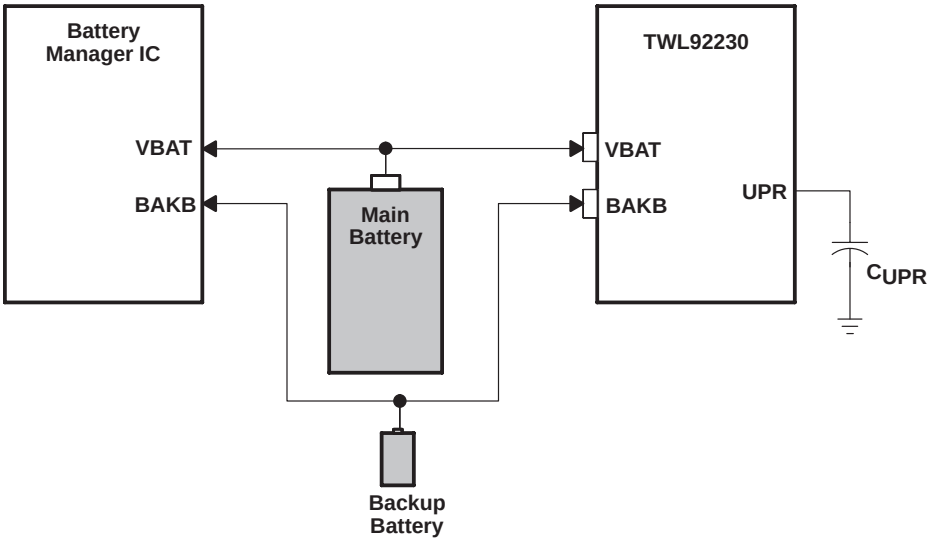


Figure 7−1. Backup Battery Connection Description

The BAKB terminal needs to be powered to correctly manage a main battery removal. If a backup battery is present in the system, it should be connected to the TWL92230, even if another component in the system already handles the RTC and the backup battery charging. Minimum current is drawn on the BAKB terminal, especially if the RTC clock is disabled in the TWL92230.

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7.2 Configuration Without a Backup Battery

If no backup battery is present in the system then the main battery can be connected to the backup battery terminal (BAKB). The typical UPR capacitor (C_{UPR}) is 1 µF.

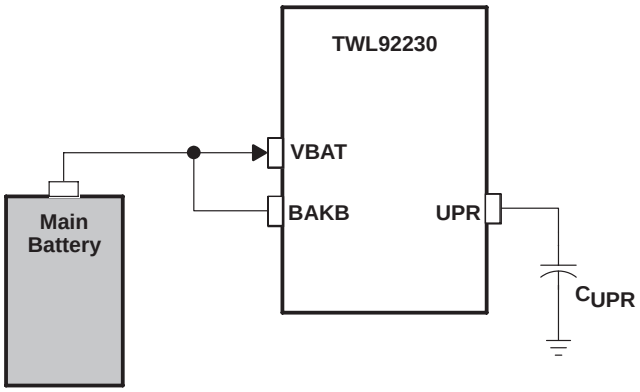


Figure 7−2. TWL92230 Without Backup Battery

7.3 Backup Battery Charger

The backup battery, in the event it is rechargeable, can be recharged from the main battery. A programmable voltage regulator powered by the main battery allows recharging of the backup battery. The backup battery charge function is enabled by setting the BBCHEN to 1 (in the BBSMS register). Charging begins when the following conditions are met:

- BBCHEN = 1
- Main battery voltage (V_{BAT}) > backup battery voltage (V_{BAKB})
- Main battery voltage> $V_{UVLO-TH}$ threshold voltage

The comparators of the BBS give the two thresholds of the backup battery charge start-up. The programmed voltage for the charger gives the end-of-charge threshold.

Table 7−1. Backup Battery Charger Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Backup battery charging current I_{BAKBCH}	V_{BAKB}= < 2.8 V, BBCHEN = 1	350	800	1000	µA
	V_{BAKB} = 0 V, BBCHEN = 1	350	800	1000	µA
End backup battery charging voltage: $V_{BAKBEND}$	$I_{VBACKUP}$ = −10 µA, BBSEL = 00	3.0	3.1	3.2	V
	$I_{VBACKUP}$ = −10 µA, BBSEL = 01	3.1	3.2	3.3	
	$I_{VBACKUP}$ = −10 µA, BBSEL = 10	2.9	3.0	3.1	
	$I_{VBACKUP}$ = −10 µA, BBSEL = 11	VBAT − 0.2	VBAT − 0.1	VBAT	
Backup battery-charger quiescent current	ON mode (BBCHEN = 1)			100	µA
	OFF mode (BBCHEN = 0)			1	
C_{UPR}		0.7	1.0	1.3	µF

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7.4 Undervoltage Lockout Detector

Undervoltage lockout with hysteresis is provided to limit battery drain. An active UVLO signal overrides all power-on mechanisms and does not allow any internal circuits except those powered by the back-up battery to be enabled. When the VBAT input voltage falls below the under-Voltage lockout threshold ($V_{UVLO-TH}$), the internal UVLO signal goes active, and after a debounce period, resets all register-based logic and disables all functions in the TWL92230 except VDIG, REFSYS, CLKGEN, RTC and debounce circuitry. The debounce period is programmable with the UVLODB_PER bits in the DETECT_CTRL register. While UVLO is active, all circuits are locked in an inactive and well-behaved state. The current drain by the TWL92230 while in this state is minimal.

Table 7−2. UVLO Detector Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparator response time				10	µs
Comparator rising-VBAT threshold ($V_{UVLO-TH}$)	Measured on VBAT terminal			2.85	V
Comparator falling-VBAT threshold ($V_{UVLO-TH}$)	Measured on VBAT terminal	2.45			V
Operating voltage (for assured functionality)	Measured on VBAT terminal, Minimum voltage for falling VBAT only	2.0		5.5	V
Comparator hysteresis			150		mV
Debouncing duration UVDB_PER[2:0] = 000			0		µs
Debouncing duration UVDB_PER[2:0] = 001			100(1)		µs
Debouncing duration UVDB_PER[2:0] = 010			200		µs
Debouncing duration UVDB_PER[2:0] = 011			300		µs
Debouncing duration UVDB_PER[2:0] = 100			400		µs
Debouncing duration UVDB_PER[2:0] = 101			500		µs
Debouncing duration UVDB_PER[2:0] = 110			600		µs
Debouncing duration UVDB_PER[2:0] = 111			700		µs

(1) Default Debounced time

7.5 Low-Battery Detector

In addition to the UVLO detector circuit, a LOWBAT detector can be used as a pre-warning that the main battery is getting low. When the LOWBAT signal is asserted, an interrupt can be generated to the application processor (when the LOWBAT_MSK bit is cleared to 0). This interrupt is an indication to the application processor that steps must be taken to reduce system power.

This comparator with voltage hysteresis provides a LOWBAT signal to the digital control system (DCS). Inside the DCS, the LOWBAT signal is time debounced for rising and falling edge transitions. The default debounce period is 100 µs and is programmable with the LBDB_PER bits in the DETECT_CTRL register. The voltage hysteresis and the time-debouncing ensure the data integrity and prevent false triggers caused by normal variations of the battery voltage, when the voltage first spikes above 3.2 V or when the voltage first spikes below 2.8 V.

To reduce current consumption, the comparator is automatically disabled in the M_Backup state (The UVLO signal is asserted)

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Table 7−3. Low-Battery Detector Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparator settling time				10	µs
Comparator rising-VBAT threshold ($V_{LOWBAT-TH}$)	Measured on VBAT terminal			3.2	V
Comparator falling-VBAT threshold ($V_{LOWBAT-TH}$)	Measured on VBAT terminal	2.8			V
Comparator hysteresis			150		mV
Debouncing duration LBDB_PER[2:0] = 000			0		µs
Debouncing duration LBDB_PER[2:0] = 001			100(1)		µs
Debouncing duration LBDB_PER[2:0] =010			200		µs
Debouncing duration LBDB_PER[2:0] =011			300		µs
Debouncing duration LBDB_PER[2:0] =100			400		µs
Debouncing duration LBDB_PER[2:0] =101			500		µs
Debouncing duration LBDB_PER[2:0] =110			600		µs
Debouncing duration LBDB_PER[2:0] =111			700		µs

(1) Default Debounced time

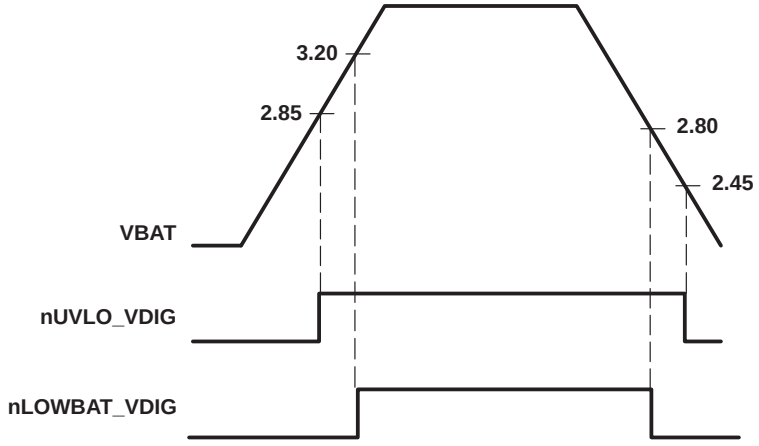


Figure 7−3. UVLO and LOWBAT Waveforms

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8 Memory Card Transceivers (MCT)

The MCT host system interfaces with the following types of removable data memory cards based on flash memory (nonvolatile memory), storing various digital data such as music, pictures, and video:

- MMC™ (Multimedia Memory Card)
- SDIO™ (Secure Digital IO devices)
- SD™ (Secure Digital memory card)
- MS™ (Memory Stick card)

8.1 Slot/Card Configurations Supported

Two separate slots (buses), Slot 1 and Slot 2, are provided for access to these multiple cards types. These two slots mainly differ in their power supplies. The intended usage of these slots is listed as follows:

1) Interfacing with one 4-bit card in Slot 1

2) Interfacing with one 4-bit card in Slot 2

3) Interfacing simultaneously with both slots using broadcast mode (limited support)

The following I^2C register bits determine which of these modes is entered.

Table 8−1. Slot/Card Configuration

REGISTER BIT	DESCRIPTION(1)
SLOT1_EN	If high, Slot 1 functionality is enabled. Default = 0.
SLOT2_EN	If high, Slot 2 functionality is enabled. Default = 0.

(1) Default debounced time

8.2 Alternate Slot Selection Option using GPIO2 Terminal

The GPIO2 pin can control the selection of either Slot 1 or Slot 2. For this alternate function, the SLOTSELEN bit must first be set to high, followed by setting both of the SLOTX_EN bits to high. Instead of entering broadcast mode (like normal), setting the SLOTSELEN bit being set allows the GPIO2 pin to control which of the two slots is enabled. See section 10.3.1 for more information.

NOTE: Note: In this mode, the GPIO2 pin can't switch between Slot 1 and Slot 2 at an infinite frequency. There is a certain minimum time (not less than 1 μsec) required between such transitions, in order for relevant circuitry to stabilize.

8.3 Slot Power Supply Configurations

Each slot has a separate configurable supply voltage, but Slot 1 must use V_{MMC}, while Slot 2 can use either V_{DCDC3} or V_{AUX} or an external supply. See the electrical specifications for MCTs as well as specifications for V_{DCDC3}, V_{AUX}, and V_{MMC} to determine all voltage combinations. All application processor communications are at V_{IO_1P8} level. A slot can be powered yet not selected. Table 8−2 summarizes the maximum current that can be consumed by cards/devices connected to Slot 1 and Slot 2.

Table 8−2. Slot 1 and Slot 2 Maximum Current

SLOT	MAXIMUM CURRENT
Slot 1	200 mA using V_{MMC}
Slot 2	400 mA using V_{DCDC3} 200 mA using V_{AUX}

The power supply chosen for Slot 2 must be shorted to the VMCS2 pin. Also, the following register bit must be set prior to powering the selected supply. This register bit is defined as follows:

Table 8−3. Slot 2 Power Supply

REGISTER BIT	DESCRIPTION
VS2_SEL[1:0]	00: SLOT2 is powered by DCDC3 (Default = 00) 01: SLOT2 is powered by VAUX 1x: SLOT2 is powered by an external source

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8.4 Additional ESD Requirements

A separate ESD protection device is required for each slot in order to adhere to IEC 61000-4-2 Level 4 specifications. Such an ESD device is typically inserted between the TWL92230 slot pins and the slot interface and may contain EMI filtering.

NOTE: The series resistance of such an ESD/EMI device will increase the effective rise/fall time from what is stated in the MCT electrical specifications table.

8.5 Broadcast Mode

Broadcast mode is accomplished by broadcasting identical information to both Slot 1 and Slot 2. This mode also has an option to send a digital AND of Slot 1 and Slot 2 signals back to the application processor. Due to the inherent simplicity of this optional function, it has limited support. The specific application of this mode defines its usefulness.

In broadcast mode, clock feedback is always sampled from Slot 1. There is no software option in place to alter this. As such, any parameter difference between Slot 1 and Slot 2, such as a difference in C_L or slot operation voltage, could define the usefulness of this mode. Also, communication protocols operating with active high signals limit the usefulness of this mode, due to the digital AND topology that is used.

8.6 Programmable Buffer Drive Strength

The drive strength of the application processor, Slot 1, and Slot 2 output buffers is I^2C register programmable:

Table 8−4. Buffer Drive Strength

REGISTER BIT	DESCRIPTION
APBUFDRV	TWL92230 to application processor output buffer strength: 1 = 3 ns/10 pF 0 = 6 ns/10 pF (default)
S1BUFDRV	TWL92230 to Slot 1 output buffer strength: 1 = 3 ns/30 pF 0 = 6 ns/30 pF (default)
S2BUFDRV	TWL92230 to Slot 2 output buffer strength: 1 = 3 ns/30 pF 0 = 6 ns/30 pF (default)

8.7 Open-Drain Capability for S1/S2 CMD

The output buffers for the MC.S2CMD and MC.S1CMD lines can be configured for open-drain communication, as opposed to the normal push-pull communication used. Only the CMD lines for Slot 1 and Slot 2 have this option. The MC.APPCMD can only operate as push-pull.

Table 8−5. Output Buffer Type

REGISTER BIT	DESCRIPTION
S1_CMD_OD	TWL92230 to Slot 1 output buffer type for MC.S1CMD: 1 = Open drain 0 = Push/pull (default = 0)
S2_CMD_OD	TWL92230 to Slot 2 output buffer type for MC.S2CMD: 1 = Open drain 0 = Push/pull (default = 0)

8.8 Output Buffer High Impedance Mode

The output buffers are forced into a high impedance state depending on which direction the data flows (either from application processor to Slot 1 and/or Slot 2, or from Slot 1 and/or Slot 2 to the application processor). This allows for bidirectional bus flow, preventing bus contention.

High Impedance is only achievable for the CMD and DAT<3:0> pin output buffers. This mode is achieved depending upon both which slots are enabled as well as the status of the relevant DIR directional control pin.

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Note: A state of true high impedance for the relevant output buffer will not occur until the supply for the relevant output buffer is fully on and regulating. This applies for output buffers associated with the Application Processor, Slot 1, and Slot 2.

8.9 Functionality Table

Table 8−6 describes general functionality of the TWL92230 MCTs, via I^2C and pin control.

Table 8−6. MCT Functionality

PINS	I^2C/GPIO2 CONTROL		PIN CONTROL		MODE	OPERATION
	SLOT 1 SELECTED	SLOT 2 SELECTED	CMD_DIR	DATA_ DIR[3:0]		
CLK	0	0	−	−	None	Slot 1 (CLK) and Slot 2 (CLK) forced low, App (CLKF) forced low
	1	0	−	−	Access Slot 1	App (CLK) to Slot 1 (CLK), Slot 1 (CLK) to App (CLKF), Slot 2 (CLK) forced low
	0	1	−	−	Access Slot 2	App (CLK) to Slot 2 (CLK), Slot 2 (CLK) to App (CLKF), Slot 1 (CLK) forced low
	1	1	−	−	Broadcast	App (CLK) to both Slot 1 (CLK) and Slot 2 (CLK), Slot 1 (CLK) to App (CLKF)
DATA	0	0	−	−	None	All DATA I/Os are high Z (isolation mode)
	1	0	−	L	Read Slot 1	Slot 1 (DAT0-3) to App (DAT0-3), Slot 2 (DAT0-3) are high Z
	1	0	−	H	Write Slot 1	App (DAT0-3) to Slot 1 (DAT0-3), Slot 2 (DAT0-3) are high Z
	0	1	−	L	Read Slot 2	Slot 2 (DAT0-3) to App (DAT0-3), Slot 1 (DAT0-3) are high Z
	0	1	−	H	Write Slot 2	App (DAT0-3) to Slot 2 (DAT0-3), Slot 1 (DAT0-3) are high Z
	1	1	−	L	Broadcast read	Slot 1 (DAT0-3) AND Slot 2 (DAT0-3) to App (DAT0-3) [logical AND]
	1	1	−	H	Broadcast write	App (DAT0-3) to both Slot 1 (DAT0-3) and Slot 2 (DAT0-3)
CMD	0	0	−	−	None	All CMD I/Os are high Z (isolation mode)
	1	0	L	−	Read Slot 1	Slot 1 (CMD) to App (CMD), Slot 2 (CMD) is high Z
	1	0	H	−	Write Slot 1	App (CMD) to Slot 1 (CMD), Slot 2 (CMD) is high Z
	0	1	L	−	Read Slot 2	Slot 2 (CMD) to App (CMD), Slot 1 (CMD) is high Z
	0	1	H	−	Write Slot 2	App (CMD) to Slot 2 (CMD), Slot 1 (CMD) is high Z
	1	1	L	−	Broadcast read	Slot 1 (CMD) AND Slot 2 (CMD) to App (CMD) [logical AND]
	1	1	H	−	Broadcast write	App (CMD) to both Slot 1 (CMD) and Slot 2 (CMD)

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8.10 Graphical Representation of MCT System

In Figure 8−1, inputs are left, outputs are right, supplies are top, and grounds are bottom, except for cases of bidirectional I/O. The external IEC ESD component is mandatory. Figure 8−1 illustrates mainly the voltage transceiver function.

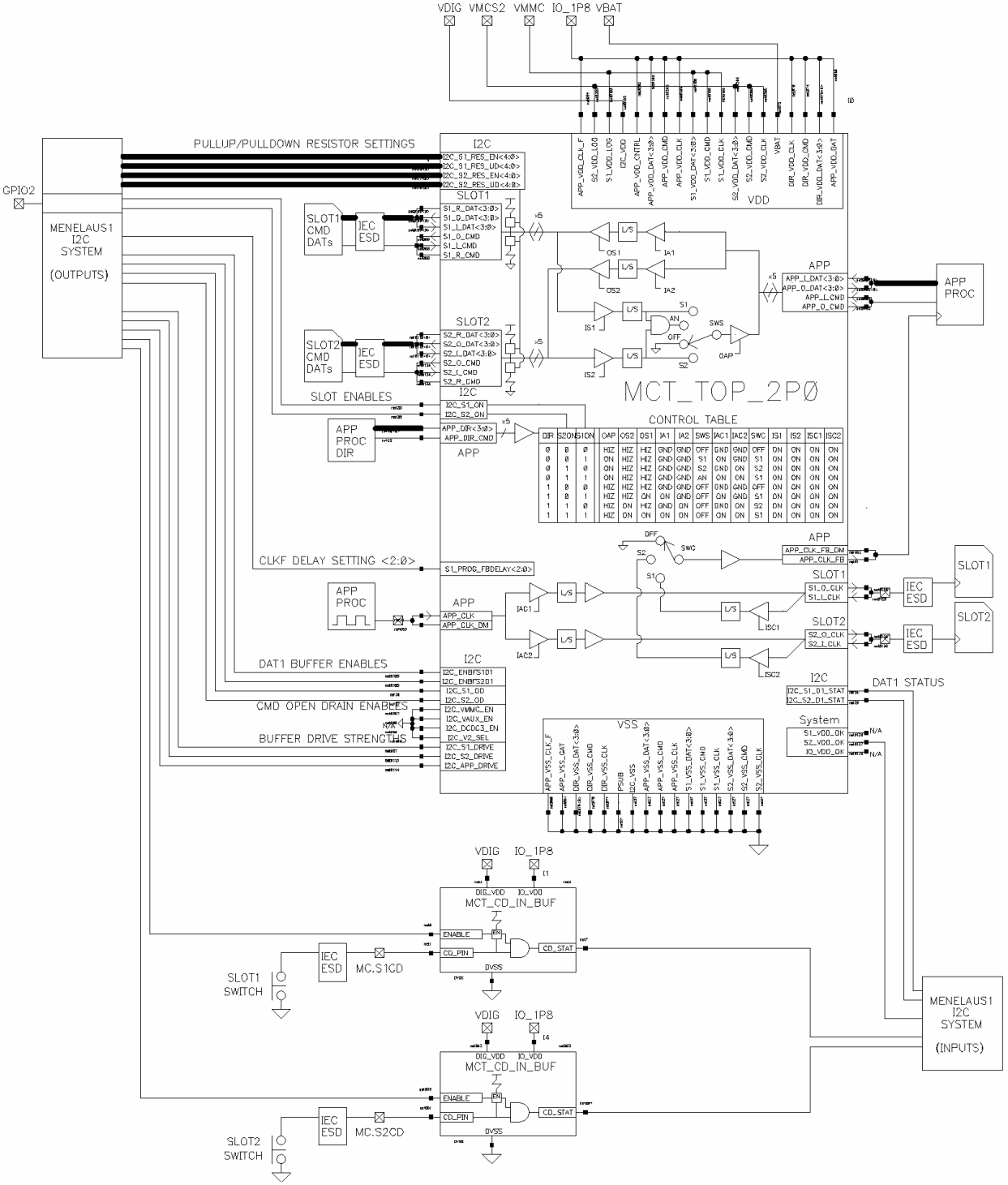


Figure 8−1. Graphical Representation of MCT System

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8.11 Nonoptimized System Usages

Various hardware operations and functionalities may be possible but are not optimized for use with this system.

8.11.1 8-Bit Data Cards

When using an 8-bit data card, only 4 bits maximum of communication are supported.

8.11.2 SD Write Protect

When needing to monitor the SD Card write-protect key, one must identify a solution external to this system, such as using a combination of spare system input pin, pullup resistor, and debounce circuitry.

8.11.3 Parallel Card Use

Using parallel cards across either Slot 1 or Slot 2 is not recommended. This design may not fully support such an arrangement, depending on reliability and speed requirements, related to insertion/removal of multiple cards. This design does not offer a separate card detect for each such parallel card. This design does include an I^2C selectable mode for CMD open drain communication, which is required for parallel card access. The insertion of an additional discharged card into a slot already communicating with another card may result in temporary loss of power to both cards, depending on the capacitance of the card and the supply. Complete functionality is only assured when the system uses a single card per slot.

8.11.4 Nontransceiver Slot Use

If a slot is not used for communication with a memory card, no special design consideration is in place to allow various unused pins to be used for other functions. One possibly useful scenario would be to level shift signals between V_{S2} and V_{IO_1P8} (with either $V_{S2} = V_{DCDC3}$ or $V_{S2} = V_{AUX}$), but all associated Slot 2 signals continue to operate as if a memory card is in use (including card detect, interrupt generation, slot power control, etc.). Such use must be well understood and characterized by the customer in a given consumer application.

8.11.5 Connections When No Power Applied to Slots

TWL92230 was designed such that when no power is applied to either Slot 1 or Slot 2, but power is applied to IO_1P8, all relevant MCT pins can be floating (except for power, ground, MC.S1CD and MC.S2CD have internal 100k resistor pullup to IO_1P8 hence can be left floating), without causing any noticeable change to various functional and/or parametric requirements (provided that relevant I^2C bits are correctly set). For example, when measuring the overall current consumption of TWL92230, one should not need to tie various MCT pins either hi/lo (leaving them floating should be OK).

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8.12 Onboard Communication Pullup/Pulldown Resistors

The TWL92230 includes many optional I^2C enabled internal pullups and pulldowns for CMD and DAT lines.

NOTE: Setting the SLOT1_EN and SLOT2_EN bits is not required to have pullup/pulldown functionality.
When using external ESD/EMI device, these pullup/pulldowns will not be connected directly to the card slot.
The pullup resistor will not be fully enabled until the supply for the relevant pullup resistor is fully on and regulating. This applies to the Slot 1 and Slot 2 power supplies. The pulldown resistor has no such limitations.

The following are for Slot 1:

Table 8−7. Register Bits for Slot 1

REGISTER BIT	DESCRIPTION
S1_CMD_EN	1 = Enable pullup/pulldown on MC.S1CMD pin
S1_DAT3_EN	1 = Enable pullup/pulldown on MC.S1DAT3 pin
S1_DAT2_EN	1 = Enable pullup/pulldown on MC.S1DAT2 pin
S1_DAT1_EN	1 = Enable pullup/pulldown on MC.S1DAT1 pin
S1_DAT0_EN	1 = Enable pullup/pulldown on MC.S1DAT0 pin
S1_CMD_UP	For MC.S1CMD pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected
S1_DAT3_UP	For MC.S1DAT3 pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected
S1_DAT2_UP	For MC.S1DAT2 pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected
S1_DAT1_UP	For MC.S1DAT1 pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected
S1_DAT0_UP	For MC.S1DAT0 pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected

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Similar pullup/pulldown bits for Slot 2 are shown below:

Table 8−8. Register Bits for Slot 2

REGISTER BIT	DESCRIPTION
S2_CMD_EN	1 = Enable pullup/pulldown on MC.S2CMD pin
S2_DAT3_EN	1 = Enable pullup/pulldown on MC.S2DAT3 pin
S2_DAT2_EN	1 = Enable pullup/pulldown on MC.S2DAT2 pin
S2_DAT1_EN	1 = Enable pullup/pulldown on MC.S2DAT1 pin
S2_DAT0_EN	1 = Enable pullup/pulldown on MC.S2DAT0 pin
S2_CMD_UP	For MC.S2CMD pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected
S2_DAT3_UP	For MC.S2DAT3 pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected
S2_DAT2_UP	For MC.S2DAT2 pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected
S2_DAT1_UP	For MC.S2DAT1 pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected
S2_DAT0_UP	For MC.S2DAT0 pin, 0 = Pulldown resistor selected 1 = Pullup resistor selected

8.13 DAT1 Interrupt Support

For devices/cards of Slot 1 and/or Slot 2 where DAT_1 can be used to generate an interrupt, support is included for this via relevant I^2C registers and the INT pin of TWL92230. The design of the I^2C system will be such that only an unselected, powered slot with such a device can generate this interrupt, provided that this option is selected by the application software (this interrupt function enabled). For such a case, the individual IRQ status is set to active (HIGH) when there is a low (GND) level on DAT1, that will be level sensitive (instead of edge sensitive) and not debounced. The IRQ status changes to inactive (LOW) when this interrupt function is disabled. All such interrupts are to be asynchronous. The register bits associated with this interrupt generation function are described below:

Table 8−9. DAT1 Interrupt Raw

REGISTER BIT	DESCRIPTION
S1_DAT1_ST	Mirrors the raw state on the MC.S1DAT1 pin
S2_DAT1_ST	Mirrors the raw state on the MC.S2DAT1 pin

Table 8−10. DAT1 Interrupt Mask

REGISTER BIT	DESCRIPTION
S1D1_MSK	Mask for Slot1 MC.S1DAT1 interrupt
S2D1_MSK	Mask for Slot2 MC.S2DAT1 interrupt

Table 8−11. DAT1 Interrupt Output

REGISTER BIT	DESCRIPTION
S1D1	High if a MC.S1DAT1 interrupt event occurred on Slot 1
S2D1	High if a MC.S2DAT1 interrupt event occurred on Slot 2

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This special DAT1 interrupt functionality is enabled by a combination of the SLOTx_EN bits along with the required setting of the following bits:

Table 8−12. DAT1 Input Buffer Enable

REGISTER BIT	DESCRIPTION
S1D1_BUFEN	If 1, it forces the MC.S1DAT1 input buffer always on even when Slot 1 is disabled (default=0)
S2D1_BUFEN	If 1, it forces the MC.S2DAT1 input buffer always on even when Slot 2 is disabled (default=0)

NOTE: S1D1_BUFEN and S2D1_BUFEN bits should be set active only when the relevant Slot 1 or Slot 2 supply is fully on and regulating, in order to prevent false interrupts. S1D1_BUFEN and S2D1_BUFEN bits should never be set active in a consumer application that uses active-high bus notation, in order to prevent false interrupts. This function is designed for use only with active-low bus notation. S1D1_BUFEN and S2D1_BUFEN bits allows for multiple card types to be supported.

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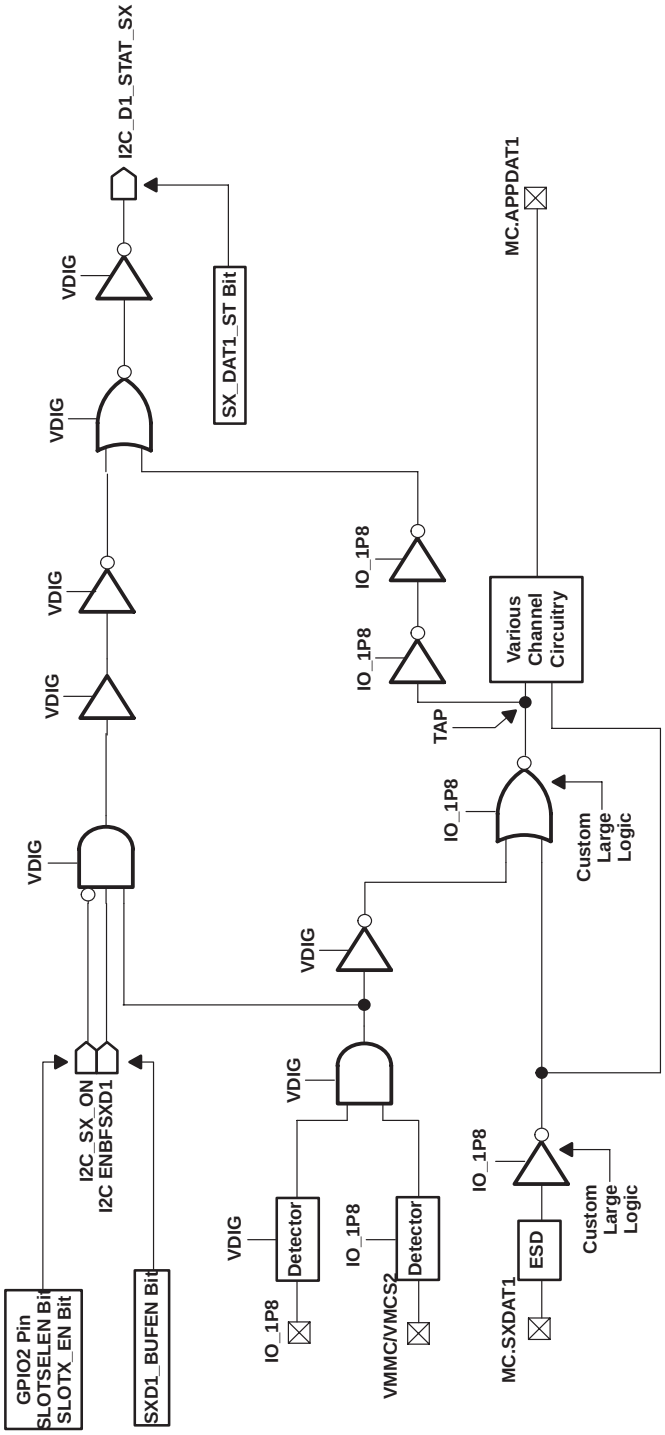


Figure 8−2. DAT1 Input Buffer

8.14 Considerations for Desired Functionality

8.14.1 Power Sequence

This design assumes that V_{MCS1} is greater or equal to V_{IO_1P8} for normal Slot 1 operation; likewise, V_{MCS2} is greater or equal to V_{IO_1P8} for normal Slot 2 operation. Also, since V_{IO_1P8} level controls many transceiver operations, V_{IO_1P8} must be powered on before V_{MCS1} and/or V_{MCS2}. Similarly, V_{MCS1} and/or V_{MCS2} must be powered off before V_{IO_1P8} is powered off, or undesired operation may result.

8.14.2 Slot Supply Rise/Fall

For both Slot 1 and Slot 2, the rise/fall time of the supply depends on the properties of the power supply and the associated loading. Please see the specifications for V_{DCDC3}, V_{AUX}, and V_{MMC} in order to determine these rise/fall times.

8.15 Special Design Considerations

8.15.1 Signal Skew Minimization

The transceivers are designed in such a way to match CMD/CLK/DAT line properties, while maintaining certain functional differences among these signals. This is to minimize skew between signals. Note: Directional control does not require such matching among communication channels.

8.15.2 Matching Slot 1 vs Slot 2

To maximize broadcast mode effectiveness, special design considerations are in place to match Slot 1 vs Slot 2.

8.16 Transceiver Delay and Skew

The difference between the propagation delay of data and clock is reduced by using an internal delayed clock feedback to the application processor. However, since the device will be placed between TWL92230 and the Memory Card, the propagation delays are not fully cancelled out, and the data will lag the clock approximately by 2 times the propagation delay of this device (see Figure 8−3). The propagation delay is minimized to allow for quick back-and-forth operations such as with a read command. In the following table, propagation delays from low to high (t_{PLH}) and from high to low (t_{PHL}) are assumed as the time from 50% of input supply to 50% output supply. Figure 8−3 assumes 0-ns setting for the application clock feedback programmable delay. See Table 8−13 for details.

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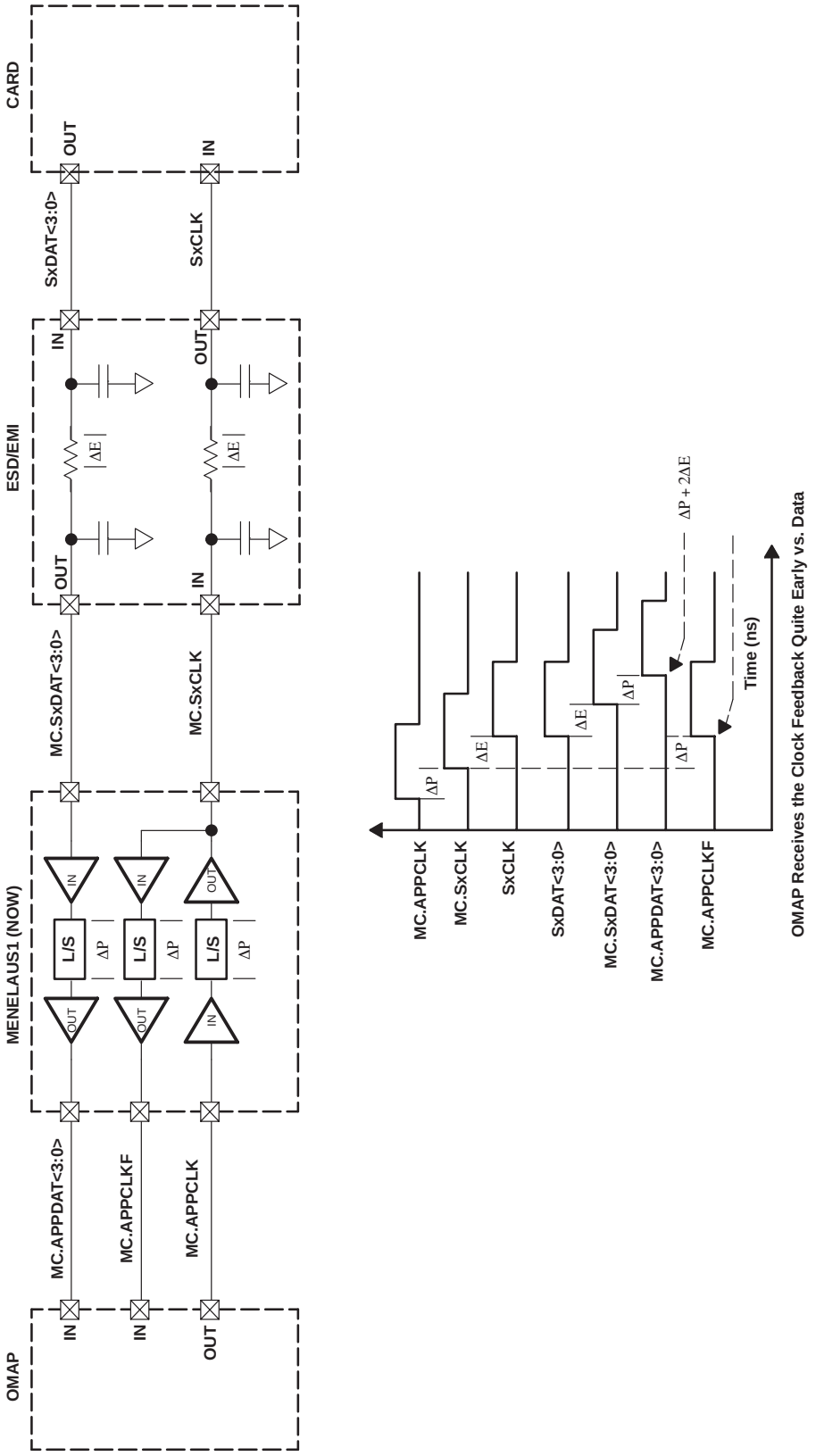


Figure 8−3. Diagram for MCT Data and Clock Delays

Table 8−13. Propagation Delays

PARAMETER	CATEGORY	FROM (INPUT)	TO (OUTPUT)	MAX	UNIT
t_{PZH} (t_{en})	Enable delay	DIR terminal	App Processor	8	ns
t_{PZL}(t_{en})	Enable delay	DIR terminal	App Processor	8	ns
t_{PZH} (t_{en})	Enable delay	DIR terminal	Slot Buffer	8	ns
t_{PZL} (t_{en})	Enable delay	DIR terminal	Slot Buffer	8	ns
t_{PHZ} (t_{dis})	Disable delay	DIR terminal	App Processor	8	ns
t_{PLZ} (t_{dis})	Disable delay	DIR terminal	App Processor	8	ns
t_{PHZ} (t_{dis})	Disable delay	DIR terminal	Slot Buffer	8	ns
t_{PLZ} (t_{dis})	Disable delay	DIR terminal	Slot Buffer	8	ns
$t_{sk(o)}$	Skew	App Processor	Slot Buffer	0.5	ns
t_{PLH} (t_{pd})	Propagation delay	App Processor to TWL92230 to App Processor		7.5	ns
t_{PHL} (t_{pd})	Propagation delay	App Processor to TWL92230 to App Processor		7.5	ns
t_{PLH} (t_{pd})	Propagation delay	TWL92230 to App Processor to TWL92230		7.5	ns
t_{PHL}(t_{pd})	Propagation delay	TWL92230 to App Processor to TWL92230		7.5	ns

8.17 Application Processor Interface Electrical Specifications

Table 8−14. Application Processor Interface Electrical Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply for drivers			$V_{IO\ 1P8}$		V
Operation frequency for clock line				52	MHz
Rise/fall time at the input	For 52-MHz operation, 10% to 90% , 90% to 10%		3		ns
Rise/fall time (APBUFDRV = 0)	10% to 90% , 90% to 10% (C_L = 10 pF)			6	ns
Rise/fall time (APBUFDRV = 1)	90% to 10%, 90% to 10% (C_L = 10 pF)			3	ns
Time high (SxBUFDRV = 1), CLK	90% to 90% (at 52MHz) (C_L = 10 pF)	6.5			ns
Time Low (SxBUFDRV = 1), CLK	10% to 10% (at 52MHz) (C_L = 10 pF)	6.5			ns

8.18 Memory Card Interface Electrical Specifications

Table 8−15. Memory Card Interface Electrical Specifications

PARAMETER	PARAMETER	MIN	TYP	MAX	UNIT
Power supply for slot (V_{MCS})		1.7		3.2	V
Pullup resistance for CD (R_{PU_CD})		50	100	150	kΩ
Pullup resistance for CMD (R_{PU_CMD})		10	20	100	kΩ
Pullup resistance for DAT0-3 (R_{PU_DAT})		50	75	100	kΩ
Pulldown resistance for CMD (R_{PD_CMD})		50	125	200	kΩ
Pulldown resistance for DAT0-3 (R_{PD_DAT})		50	125	200	kΩ
Operation frequency for clock line				52	MHz
Rise/fall time at the input	For 52 MHz operation, 10% to 90% , 90% to 10%		3		ns
Rise/fall time (SxBUFDRV = 0)	10% to 90%, 90% to 10% (C_L = 30pF, neglecting system resistance)			6	ns
Rise/fall time (SxBUFDRV = 1)	10% to 90%, 90% to 10% (C_L = 30pF, neglecting system resistance)			3	ns
Time high (SxBUFDRV = 1), CLK	90% to 90% (at 52 MHz) (C_L = 30pF, neglecting system resistance)	6.5			ns
Time low (SxBUFDRV = 1), CLK	10% to 10% (at 52 MHz) (C_L = 30pF, neglecting system resistance)	6.5			ns

Note on Series Resistance:

Any series resistance between the Memory Card and the TWL92230 can increase the rise/fall times for output buffers shown in Table 8−15. This can also affect Time High and Time Low.

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Note on Load Capacitance

The 30 pF specified for drive strength was determined based on using a single card and complying with the ESD specifications of IEC 61000-4-2 Level 4 requirements. The derivation is as follows:

C_L is the maximum external capacitance load for the MCT drivers and also for the Memory Card Drivers.

For example C_L = 30 pF = 7 pF (card or host) + 20 pF (ESD protection) + 3 pF (PWB+connector)

Note on Line Inductance

Minimization of line inductance on board layout is critical to meet high-speed standards and reduce ringing and reflections.

Note on Typical Rise/Fall Time

Due to the output driver design, the typical rise/fall time is about 30% faster when using the maximum specified slot power voltage, as opposed to using the minimum specified slot power voltage.

Note on connections when memory card transceivers are not used

MC.S1DAT0, MC.S1DAT1, MC.S1DAT2, MC.S1DAT3, MC.S1CMD, and MC.S1CLK can be left floating or grounded when Slot1 is not used. MC.S1CD can be left floating as it has an internal pullup resistor.

MC.S2DAT0, MC.S2DAT1, MC.S2DAT2, MC.S2DAT3, MC.S2CMD, and MC.S2CLK can be left floating or grounded, and VMCS2 should be grounded, when Slot2 is not used. MC.S2CD can be left floating as it has an internal pullup resistor.

When SLOT1_EN and SLOT2_EN bits are not active, MC.APPCLK, MC.APPDAT<3:0>, MC.APPCMD, APPDIR<3:0> and MC.APPCDIR are allowed to float without causing any leakage current problem.

8.19 Card Detect Behavior

Two pins are provided on the TWL92230 for card detection of Slot 1 and Slot 2. These pins are assumed to interface with a SPST (single-pole single-throw) mechanical switch, which can be either NO (normally open) or NC (normally closed).

Table 8−16. Card Detect Behavior

REGISTER BIT	DESCRIPTION
S1CD_SWNO	Set to high if card detect switch of Slot 1 is normally open. Default = 1.
S2CD_SWNO	Set to high if card detect switch of Slot 2 is normally open. Default = 1.

A 100-kΩ internal pullup resistor is permanently connected to the V_{IO_1P8} supply. The I2C register of S1CD_BUFEN and S2CD_BUFEN are not being used. There are two internal signals (S1CD_ST or S2CD_ST) which will respond directly to the logical levels of MC_S1CD and MC_S2CD pins respectively. These pins are assumed to be connected to an external switch capable of driving a low resistive path to ground. Memory card detection must only be functional in M_Active and M_LowVolt modes of the TWL92230.

The I^2C system is responsible for reflecting the signals from the card detect buffer. Debouncing of the raw card detect signal is optional, depending on the setting of the SxCD_DBEN bits. The debouncing can be approximately 32 ms.

Table 8−17. Card Detect Interrupt Generation

REGISTER BIT	DESCRIPTION
S1CD_DBEN	Set to high/low for using debounced/raw state of the CDS1 pin for interrupt generation
S2CD_DBEN	Set to high/low for using debounced/raw state of the CDS2 pin for interrupt generation

A card insertion/removal can generate an interrupt to the application processor via the INT pin, provided that this functionality is enabled before such action. Interruption occurs asynchronously. Following such an interruption, the application processor can then read a status register to determine the cause. Interruption generation can be enabled separately for Slot 1 and Slot 2. Possible causes for interruptions and appropriate register bits are defined as follows:

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Table 8−18. Card Detect Interrupt Raw

REGISTER BIT	DESCRIPTION
S1_CD_ST	Mirrors the synchronized (debounced or not) state on the CDSX pin when the SxCD_BUFEN is enabled.
S2_CD_ST	Mirrors the synchronized (debounced or not) state on the CDSX pin when the SxCD_BUFEN is enabled.

Table 8−19. Card Detect Interrupt Mask

REGISTER BIT	DESCRIPTION
S1CD_MSK	Mask for Slot 1 card insertion/removal interrupt
S2CD_MSK	Mask for Slot 2 card insertion/removal interrupt

Table 8−20. Card Detect Interrupt Output

REGISTER BIT	DESCRIPTION
S1CD	High if a card insertion/removal event occurred on Slot 1
S2CD	High if a card insertion/removal event occurred on Slot 2

A card removal can asynchronously and immediately power down any of V_{DCDC3}, V_{AUX}, or V_{MMC} according to which supply is in use by the respective slots, clearing the enable register bits associated with these power supplies. If an external supply is selected to power Slot 2 (VS2_SEL=1x) then the auto power-down function of Slot 2 is disabled. All associated transceiver slot enable bits (SLOTx_EN) must also be automatically cleared. The time required for power-down would be according to the resistive pulldown strength specified for V_{DCDC3}, V_{AUX}, or V_{MMC}. The application processor can then subsequently respond once the interrupt is processed. Conversely, card insertion, will never automatically enable a power supply. This automatic power-down function is optional for each slot according to the following bit definitions:

Table 8−21. Card Removal Power Down

REGISTER BIT	DESCRIPTION
S1_AUTO_EN	If 1, bits associated with Slot 1 power supply and Slot 1 enable are cleared. Default = 0.
S2_AUTO_EN	If 1, bits associated with Slot 2 power supply (if VS2_SEL = 0x) and Slot 2 enable are cleared. Default = 0.

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8.20 MCT Slot 1 Detection

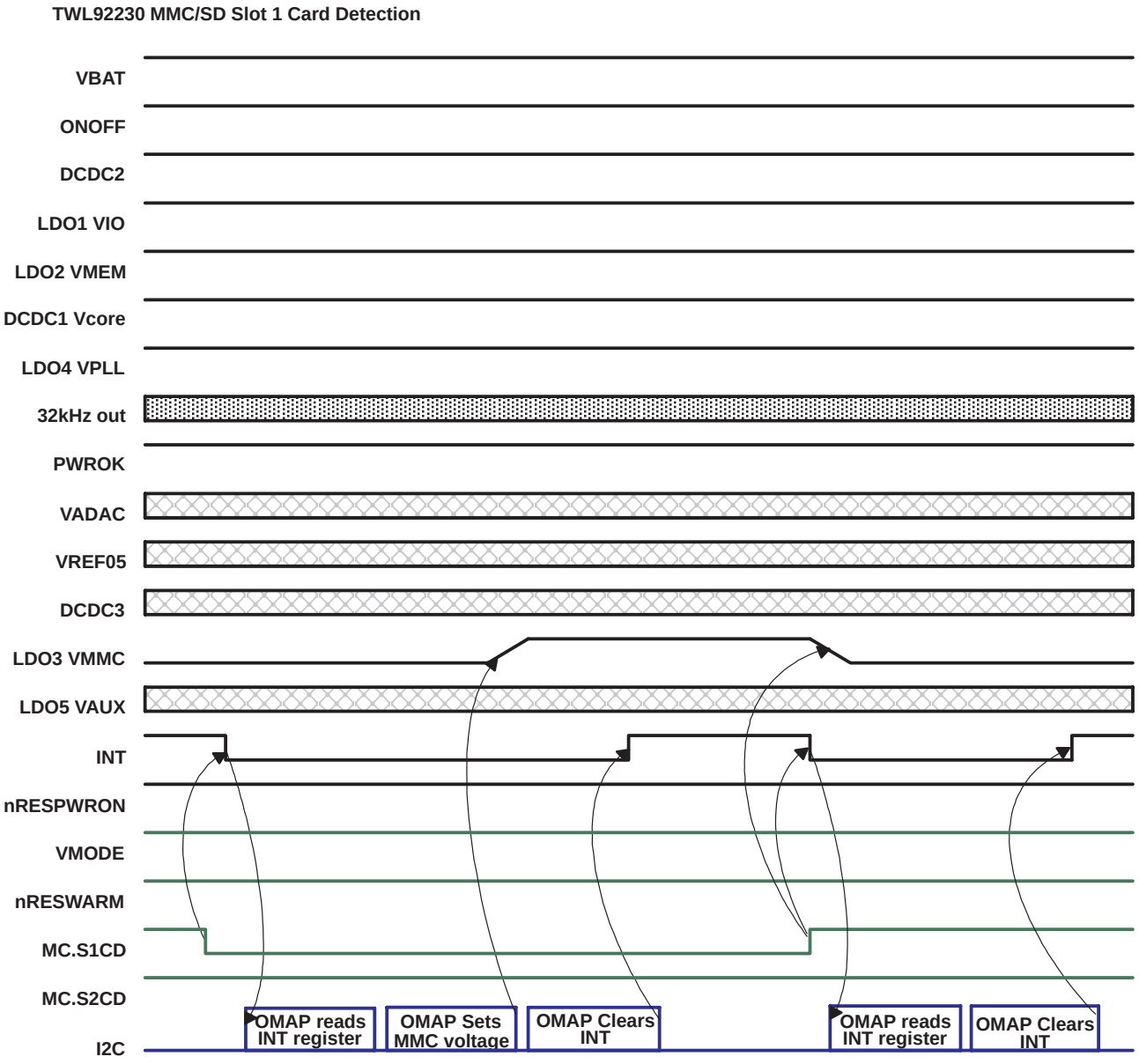


Figure 8−4. Slot 1 Card Detection

Figure 8−4 shows card detect waveforms for normally-open switches. Card detect waveforms would be inverted for normally-closed switches.

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Slot 1 Card Detection (and powered by VMMC LDO3)

Before any card insertion/removal operation is detected and an interrupt is sent to OMAP, OMAP has to set the MCT registers bits in the proper manner. That is, set the card detect switch behavior and enable the interrupt for Slot 1 card detect. For further information, see the MCT sections in this document. Once the card detection circuits are setup correctly, any change (edge) from high-to-low or low-to-high will cause an interrupt. For automatic shut down functionality, the direction (high-to-low or low-to-high) is dependent on the SxCD_SWNO setting. If SxCD_SWNO=1 (normally open switch), then a high-to-low transition on SxCD pin will cause an interrupt (indicating a card has been inserted), and a low-to-high transition will cause an interrupt (indicating a card has been removed) as well as shut down the correct regulator (depending on VS2_SEL setting) if this feature is enabled (Sx_AUTO_EN=1). If SxCD_SWNO=0 (normally closed switch), then a low-to-high transition on SxCD pin will cause an interrupt (indicating a card has been inserted), and a high-to-low transition will cause an interrupt (indicating a card has been removed) as well as shut down the correct regulator (depending on VS2_SEL setting) if this feature is enabled (Sx_AUTO_EN=1).

Card insertion:

1. MC.S1CD terminal is asserted (high or low depending on the hardware implementation, see bit S1CD_SWNO. In this example it is active low) due the card insertion
2. An interrupt is generated by the TWL92230 to OMAP
3. OMAP reads the content of TWL92230 interrupt register
4. OMAP sets the card slot voltage according to the card voltage capability (1.8 V/3.0 V).
5. OMAP clears the TWL92230 card insertion detection interrupt.

Card removal

1. MC.S1CD terminal is asserted (high or low depending on the hardware implementation, see bit S1CD_SWNO. In this example it is active high) due to the removal of the card.
2. If the S1_AUTO_EN bit is set, then TWL92230 automatically shuts down VMMC LDO3 and relevant MCT bits including SLOTx_EN. If not, then OMAP has to handle the card shutdown sequence. Note the automatic shut down feature only applies to TWL92230's regulators as there is no enable control available for external supply source.
3. An interrupt is generated by TWL92230 to OMAP.
4. OMAP reads the content of TWL92230 interrupt register.
5. OMAP clears the TWL92230 card removal detection interrupt.

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8.21 MCT Slot 2 Detection

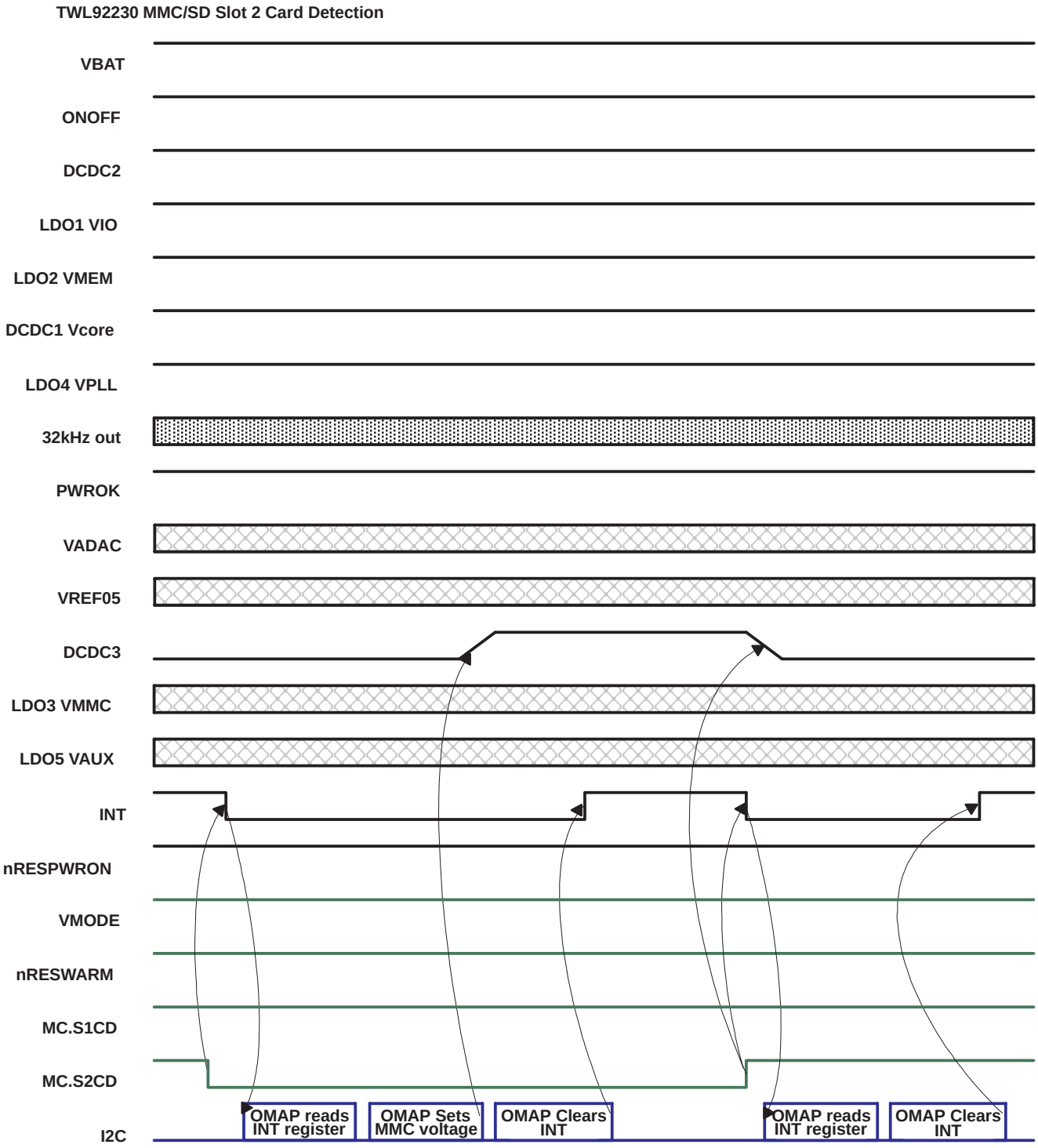


Figure 8−5. Slot 2 Card Detection (Using DCDC3)

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Slot 2 Card Detection (and powered by DCDC3 or VAUX LDO5)

Before any MMC/SD insertion/removal operation is detected and an interrupt is sent to OMAP, OMAP has to set the MCT registers bits. That is, set the card detect switch behavior and enable the interrupt for Slot 2 card detect. For further information, see the MCT sections in this document.

Slot 2 can be powered by DCDC3 or by VAUX LDO5 depending on the hardware connection that is implemented in the design. The selection in TWL92230 is made with the VS2_SEL bit in the MCT_CTRL1 register.

Card insertion

1. MC.S2CD terminal is asserted (high or low depending on the hardware implementation, see bit S2CD_SWNO. In this example, it is active low) due the card insertion.
2. An interrupt is generated by TWL92230 to OMAP.
3. OMAP reads the content of TWL92230 interrupt register.
4. OMAP set the card slot voltage according to the card voltage capability (1.8 V/3.0 V for DCDC3 or 1.8 V/2.8 V for VAUX).
5. OMAP clears the TWL92230 card insertion detection interrupt.

Card removal

1. MC.S2CD terminal is asserted (high or low depending on the hardware implementation, see bit S2CD_SWNO. In this example, it is active high) due to the removal of the card.
2. If the S2_AUTO_EN bit is set, then TWL92230 automatically shuts down DCDC3 (or VAUX) and relevant MCT bits including SLOTx_EN. If not, then OMAP has to handle the card shutdown sequence. Note the automatic shut down feature only applies to the TWL92230 regulators as there is no enable control available for external supply source.
3. An interrupt is generated by TWL92230 to OMAP.
4. OMAP reads the content of TWL92230 interrupt register.
5. OMAP clears the TWL92230 card removal detection interrupt.

If using VAUX to supply Slot 2, then the timing diagram remains the same, except that timing diagram for DCDC3 behavior is to be changed to VAUX.

8.22 Card Detect Register Configuration Sequence

Following a powerup sequence, register accesses must be made in this order:

1. The SxCD_MSK bit(s) should be cleared (written with a 0)
2. The SxCD_SWNO bit(s) found in the MCT_CTRL1 register must be programmed according to the switch type.
3. Other bits in MCT_CTRL1 can be then be programmed.
4. The MCT_CTRL2 and MCT_CTRL3 can be programmed as required.

This sequence ensures that no improper or erroneous interrupt on either of the card detect status bits. Following this sequence, any card detect interrupt will be valid. Furthermore, this sequence will work properly for cards that were already inserted before the power up sequence.

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8.23 Application Clock Feedback Programmable Delay

The clock feedback signal can be delayed to compensate for the ESD/EMI delay described in section 8.17 and Figure 8−3 . The delay can be increased in steps of 2 ns, ranging from 0 ns to 14 ns by setting the according register bits. There are 2 sets of 3 register bits, one set for each slot. When SLOT1 or broadcast mode is selected, the S1_APPCLKF_DLY setting is used. When SLOT2 is selected S2_APPCLKF_DLY setting is used.

Table 8−22. Clock Feedback Delay Control Bits

REGISTER BITS	LOCATION	DESCRIPTION
S1_APPCLKF_DLY(2:0)	0x32 D7−D5 (S1_PULL_EN)	Sets delay for slot 1 clock feedback
S2_APPCLKF_DLY(2:0)	0x34 D7−D5 (S2_PULL_EN)	Sets delay for slot 2 clock feedback

Table 8−23. Delay Settings

SX_APPCLKF_DLY(2:0)	ADDITIONAL DELAY (NS)(1)
000	0
001	2
010	4
011	6
100	8
101	10
110	12
111	14

(1) Additional delay tolerances provided here are measured in absolute percentage (non-accumulative) +50%, −32%. That is, the minimum and maximum delays for setting 101 are 6.8 μs and 15 μs, respectively.

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9 Real-Time Clock (RTC)

The real-time clock function in TWL92230 provides time and date functions for the system to a resolution of one second. The clock is referenced to the 32-kHz oscillator and is powered by the VDIG voltage regulator, allowing it to maintain time accuracy regardless of system power configuration. A block of registers in the I^2C register map allow general access to both hosts for reading time and calendar information, but a single host is allocated the ability to set the time, calendar, alarm, and timer features. To reduce current consumption, the clock will only be activated in the RTC block when RTC_EN is high or if UPDATE_TC[3:0] is between 0x0001 and 0x1000. The RTC block provides:

1. Time information (seconds/minutes/hours) in BCD code.
2. Calendar information (day/month/year/day of the week) in BCD code up to year 2099.
3. Three interrupt generation capabilities: timer (periodic at 1s / 1m / 1h / 1d cycle), input error, or alarm (at a precise time of day).
4. Wakeup stimulus to the power management system based on alarm expiration

Figure 9−1 gives an overview.

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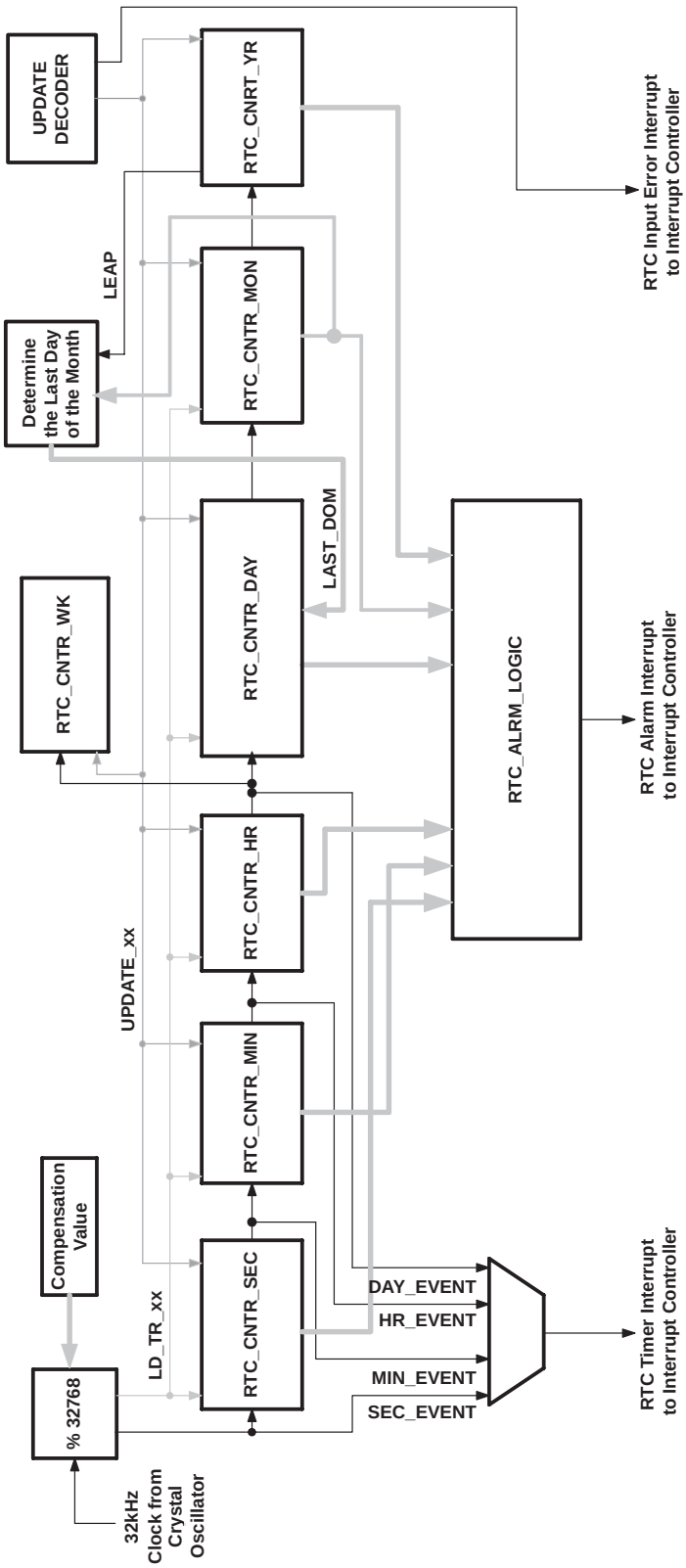


Figure 9−1. RTC Block Diagram

9.1 BCD Coding

RTC registers values are written in BCD code (binary coded decimal).

Table 9−1. BCD Coding

TIME UNIT	RANGE	REMARKS
Year	00 to 99	Leap Year : Year divisible by four Common Year : Other year
Month	01 to 12	
Day	01 to 31	01 to 31 for months 1, 3, 5, 7, 8, 10, 12 01 to 30 for months 4, 6, 9,11 01 to 29 for month 2 (leap year) 01 to 28 for month 2 (common year)
Week	00 to 06	Weekday
Hour	00 to 23	00 to 23 in 24 hours mode 01 to 12 in AM/PM mode
Minutes	00 to 59	
Seconds	00 to 59	

9.2 General Control

The RTC_EN bit of the RTC_CTRL register must only be used to completely disable the RTC function. Setting this bit low stops the 32-kHz clock input to the RTC (RTC is frozen) and reduces the overall device power consumption.

9.2.1 RTC Time and Calendar Registers

The current time and calendar registers are updated by the host processor using a simple semaphore system. To change the current settings, the desired year, month, day, hour, minute, and second are written to the RTC_YR, RTC_MON, RTC_DAY, RTC_HR, RTC_MIN, RTC_SEC registers as necessary. These parameters do not take effect immediately. Instead, they are applied simultaneously when the RTC_UPDATE register is written with an appropriate time update command. Updates can be done with the RTC either running or stopped. The RTC_UPDATE register will auto-clear after any write operation to it.

9.2.2 Interrupt Management

The RTC can generate three different interrupts:

- Timer interrupt
- Alarm interrupt
- Input Error interrupt

9.2.2.1 Timer Interrupt Management

The RTC timer event occurs periodically, either every second, minute, hour or day, on the second, minute, hour or day, depending on the EVERY[1:0] setting. When the event occurs, the RTC_TM_INT status bit is set. When enabled (RTCTMR_MSK = 0), the timer event also causes an external interrupt on the INT pin. This interrupt is active until the status bit has been cleared by writing a 1 to the RTCTMR_ACK bit (self-clearing bit).

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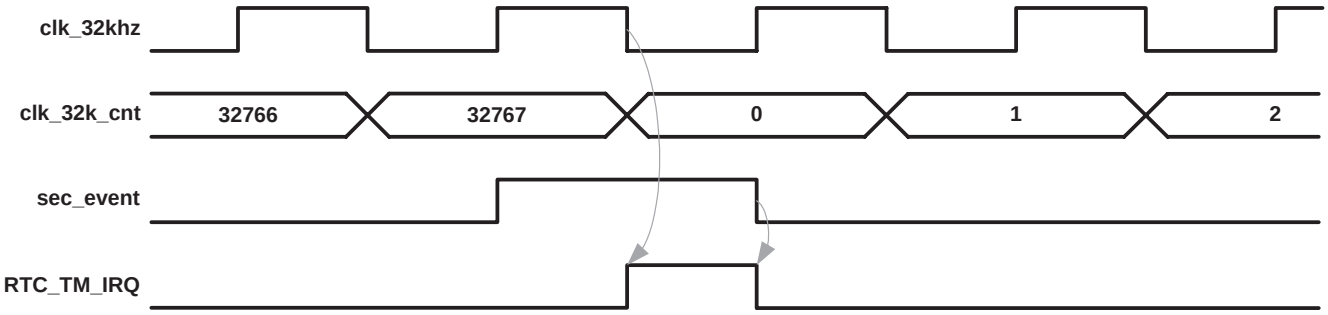


Figure 9−2. RTC Timer Interrupt

9.2.2.2 Alarm Interrupt Management

Alarm interrupts are one-time events that occur when the time specified in the RTC_AL_YR, RTC_AL_MON, … RTC_AL_SEC registers matches the current time as represented in the RTC_YR, RTC_MON, … RTC_SEC registers and when the RTC_AL_EN = 1. When this event occurs, the RTC_AL_INT status bit is set. When enabled (RTCALM_MSK = 0), the alarm event will also cause an external interrupt on the INT pin. This interrupt is active until the status bit has been cleared by writing a 1 to the RTCALM_ACK bit (self-clearing bit).

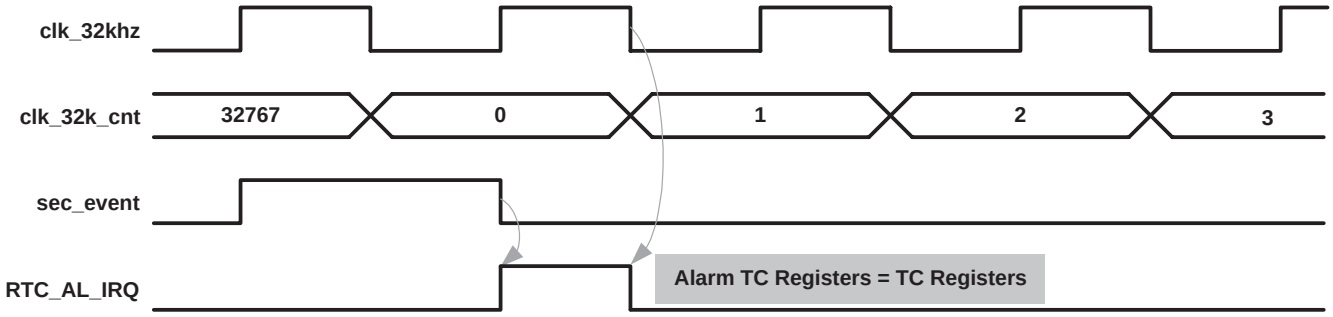


Figure 9−3. RTC Alarm Interrupt

RTC Alarm does not automatically turn ON any LDO or switchers (in M_Config_1) unless it is first in the M_WAIT_ON state (meaning that it has been transitioned from M_ACTIVE to M_WAIT_ON state by the DEVOFF bit being set to 1). For other M_Config_(0/2/3), RTC Alarm never initiates a transition to ON of the LDO and switchers (it does not initiate a transition from M_WAIT_ON to M_ACTIVE).

9.2.2.3 Input Error Interrupt Management

Input Error Interrupts are one-time events that occur when the time specified in the RTC_YR, RTC_MON, … RTC_SEC registers are inconsistent with the time calendar value during an update request. However, it does not check for RTC time inputs which are outside the valid input range specified by each of the RTC time register field. Following possible error conditions are checked by the RTC block when the RTC_ER_INT status bit is set:

- Hour input is greater than 23 (in 24 hour mode).(1)
- Month or day input = 0.
- Day input is greater than the last day of the month but less than decimal 31 (values greater than 31 are not checked).(2)
- Day input = 29 during February of a nonleap year, or day input = 30 during February of a leap year.
- Nonleap year input when month and day = February 29th.

(1) Under 12-hour mode, an hour input greater than decimal value of 12 will be interpreted as 12 hour input.
(2) A day input beyond the decimal value of 31 is currently not being checked.

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When enabled (RTCERR_MSK = 0), the error event will also cause an external interrupt on the INT pin. This interrupt is active until the status bit has been cleared by writing a 1 to the RTCERR_ACK bit (self-clearing bit).

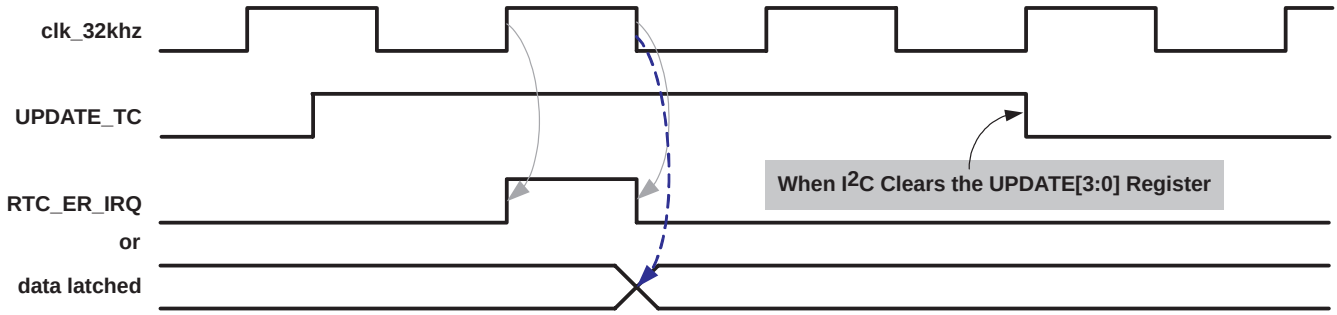


Figure 9−4. RTC Input Error Interrupt

9.3 Oscillator Drift Compensation

With the assistance of the host, TWL92230 is able to compensate for drift in the 32-kHz oscillator. To do so, the host compares the 32-kHz signal against a known reference source and calculates the needed drift compensation value (in 2s complement) versus a one-hour period and loads the value into the compensation registers:

- If the composite RTC_COMP_REG value is positive, cycles are added to the time counter.
- If the composite RTC_COMP_REG value is negative, cycles are removed from the time counter.

This process allows compensating each hour within a single 32-kHz period accuracy.

9.3.1 Compensation Registers

The RTC Compensation Registers allow fine adjustments of the RTC by adding or subtracting one or more 32-kHz clock periods every hour. The registers are written with a 2s complement value. For example, to add one 32-kHz period every hour, the host has to write 0x0001 to the RTC_COMP_MSB and RTC_COMP_LSB registers. To remove one 32-kHz period every hour, the host has to write 0xFFFF (−1) to the registers. The values 0x8000 and 0x8001 are forbidden.

These registers must not be updated during the compensation event (first second of each hour).

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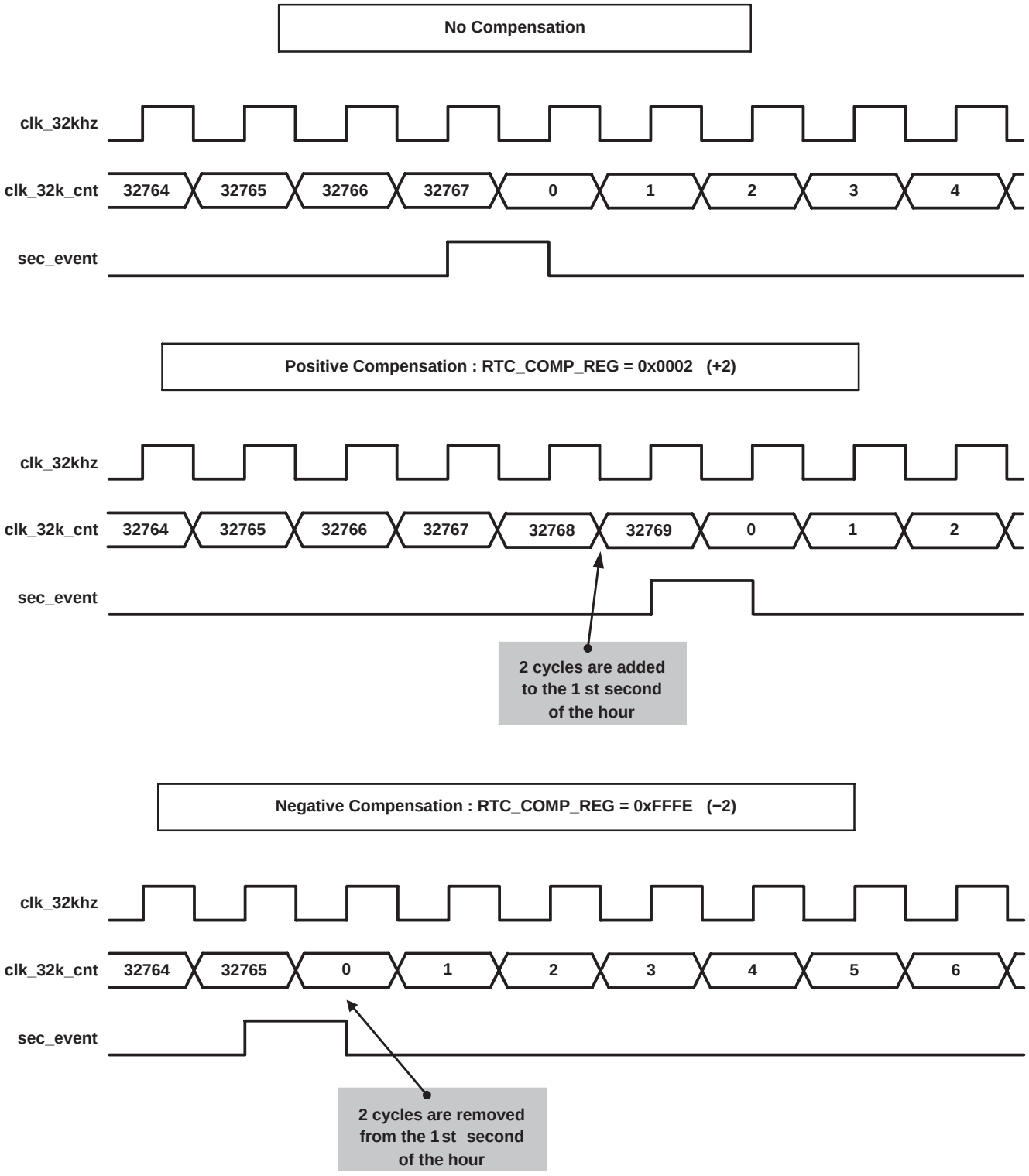


Figure 9−5. Drift Compensation Mechanism

10 Digital Control System (DCS)

10.1 Host Control Inputs

10.1.1 ONOFF

ONOFF is the signal to control the start of the boot sequence for OMAP. ONOFF can be used in default mode and in pushbutton mode and is recognized without any clock. These modes are described below.

10.1.1.1 ONOFF in Default Mode

In default mode the signal ONOFF is an input of TWL92230 that enables or disables all power to TWL92230. When high level, this input starts up TWL92230, when low level, this input shuts down TWL92230.

If the ONOFF pin is tied directly to VBAT, UPR or VDIG, the VBAT slew must be ≤5 ms to ensure a proper TWL92230 startup. If VBAT slew is >5 ms and multiple VBAT insertions occur while the ONOFF pin is tied to one of these supplies, glitches can be seen on the regulators during startup. These glitches will violate the proper startup sequence, which is required by the application processor. It is recommended that the ONOFF pin be toggled HIGH several ms after VBAT is applied.

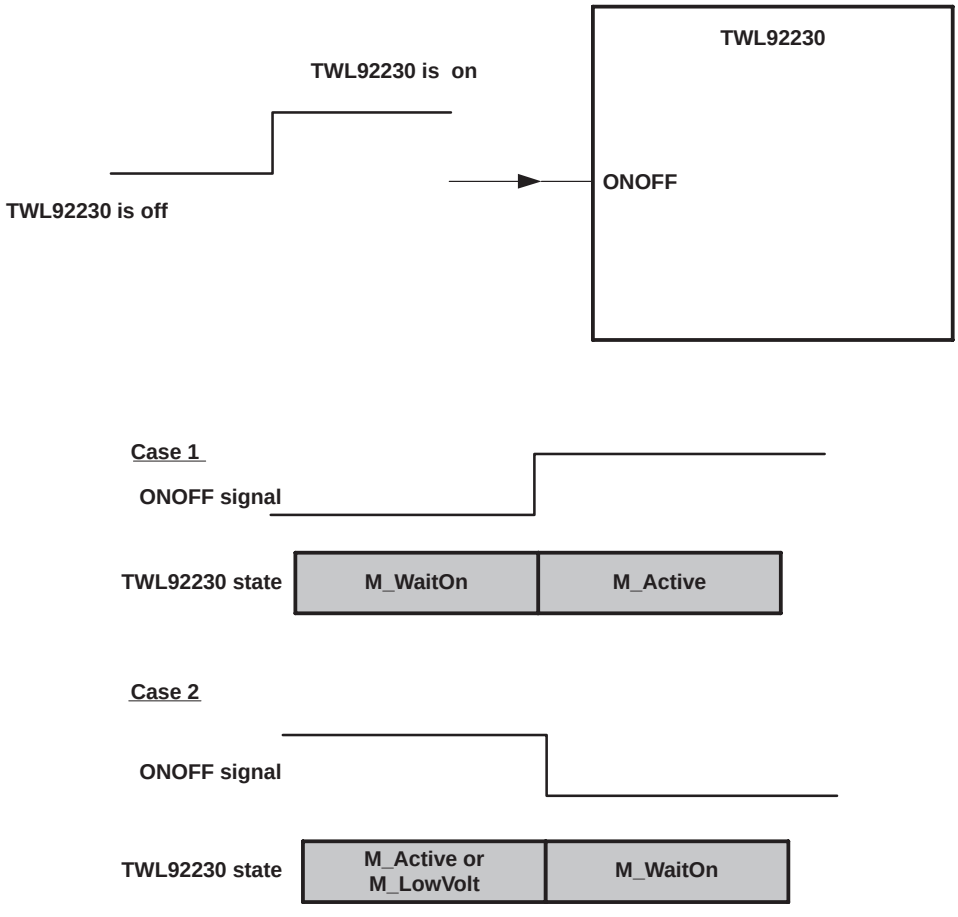


Figure 10−1. Default Mode of ONOFF Signal

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10.1.1.2 ONOFF in Pushbutton Mode

Pushbutton mode can only be used when TWL92230 is in M_Config1 (see configuration Table 10−1). In that configuration TWL92230 can manage a signal from a pushbutton as shown in Figure 10−2.

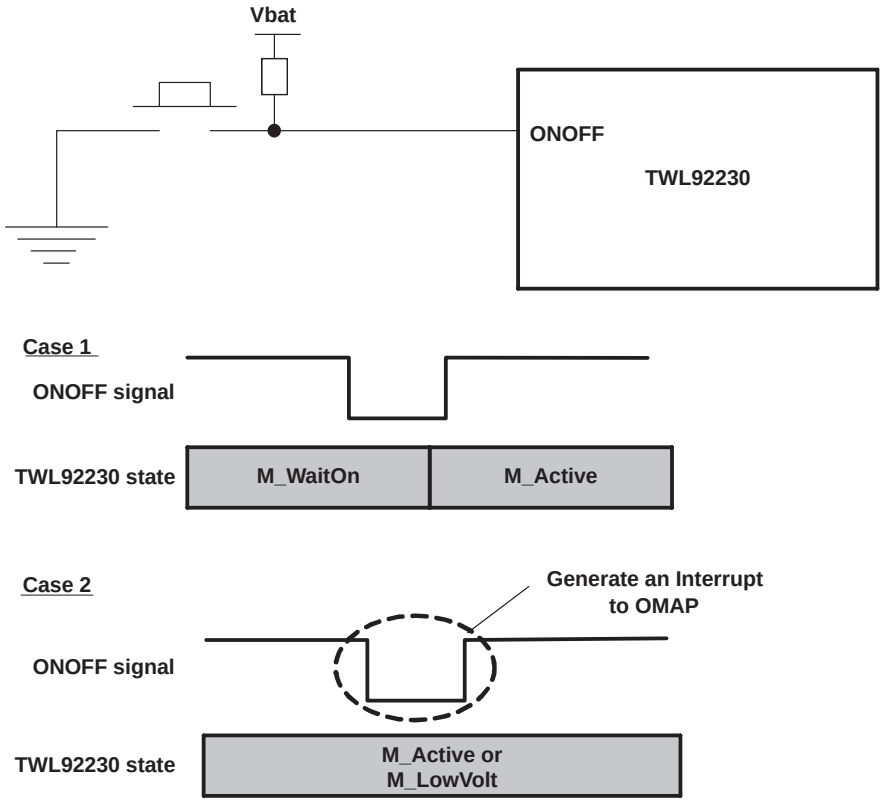


Figure 10−2. Pushbutton Mode of ONOFF Signal

This mode is different from the normal ONOFF mode because it is not symmetrical. If TWL92230 is in M_WaitOn, it starts up TWL92230, but if TWL92230 is in M_Active or M_LowVolt, it just generates an interrupt to OMAP. OMAP has then to take the decision to power down the system with software (see state machine and DEVOFF bit).

When ONOFF is used as a pushbutton, it must be debounced. The debounce time is 18600 x T_{600K}.

T_{600K} is the period of the internal 600-kHz RC oscillator.

See section 9.2.2.2 *Alarm Interrupt Management* for M_WAIT_ON to M_ACTIVE transition initiated by RTC Alarm.

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10.1.2 nRESWARM

nRESWARM is an active low input reset signal. A reset button can be connected to this line to trigger this warm reset. A peripheral or the application processor can also activate this signal by a software reset. nRESWARM is ignored until it is high at least once. In M_Config0/1/2, nRESWARM is ignored until VIO is powered up. In M_Config3, nRESWARM is ignored until DCDC2 is powered up.

SYS.nRESWARM is the matching terminal in OMAP24xx and is a combined input and open-drain output in OMAP24xx that can be directly connected to TWL92230 nRESWARM. When a nRESWARM is detected low by OMAP (even a glitch), then OMAP asserts nRESWARM low for a programmable number of 32-kHz clock cycles. On TWL92230 side, this is an input only. nRESWARM is debounced by TWL92230 (TWL92230 checks that nRESWARM is low for RESWARM_DB $\times$ 10 µs), and then will automatically restore DCDC2, VCORE, and VPLL in all M_Config modes as well as VIO and VMEM in M_Config0, M_Config1 and M_Config2 modes to their ON mode. All other resources are disabled (OFF mode), and all registers (except RTC registers and Interrupt status registers) are reset to their default value. Also, DVS hardware mode is cancelled and TWL92230 is back in software mode (HW_nSW = 0).

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10.1.2.1 nRESWARM (M_Config0, 1, 2 and 3*)

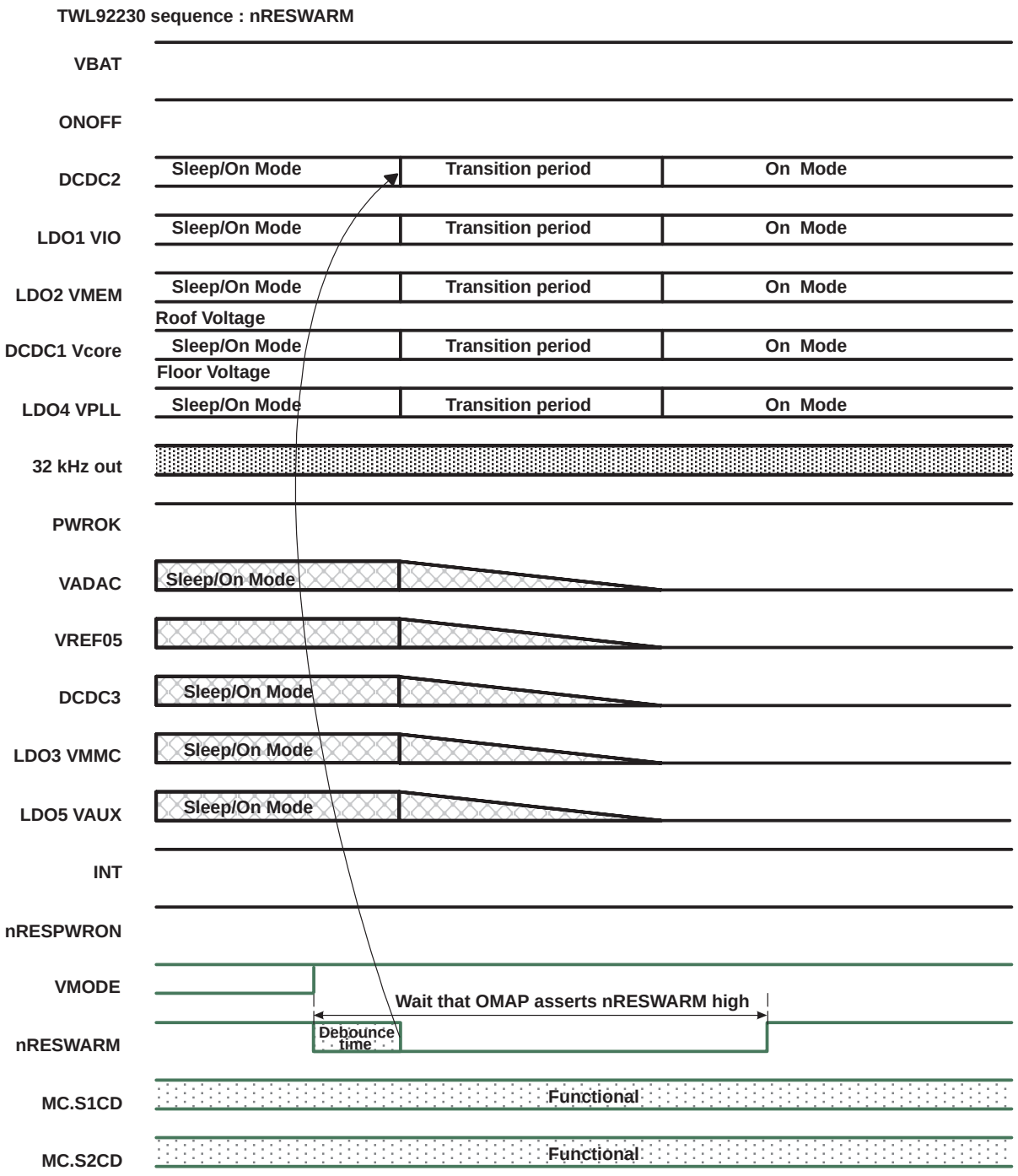


Figure 10−3. nRESWARM

Figure 10−3 applies for M_Config0 and 2. For M_Config1, the ONOFF pin will be asserted Low (see section 10.6 for Pushbutton operation). For M_Config3, VIO and VMEM LDOs are disabled. See Table 10−5 for details.

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10.1.2.2 nRESWARM Action on TWL92230

nRESWARM is an input of TWL92230. When a low signal is detected on nRESWARM by OMAP24xx, then OMAP24xx starts its warm reset sequence. OMAP24xx maintains nRESWARM low for a programmed number of 32-kHz cycles before releasing it.

When TWL92230 detects that nRESWARM goes low, then:

1. TWL92230 debounces this signal using the time defined by the RESWARM_DB bits in the DEBOUNCE1 register (see register description details for more information)
2. Once nRESWARM is debounced, the TWL92230 restores the DCDC2, VMEM, VIO, VCORE and VPLL resources to the ON mode if in M_Config0/1/2 boot mode, or DCDC2, VCORE and VPLL if in M_Config3 boot mode. All other regulators are shut down and all registers (except the RTC and INT_STATUS registers) are reset to their default values.
3. All regulator voltage settings go back to their default value. For DCDC2, this is dependent on the boot mode (see DCDC2_MODE register description).

   NOTE: The time that OMAP24xx is maintaining the nRESWARM signal asserted low must be long enough for TWL92230 to complete its sleep-to-On mode transition

10.1.3 VMODE

The VMODE input can be used to scale the VCORE voltage. This function is enabled by setting the register bit HW_nSW to 1. The VMODE input can also be used to force regulators from the ON mode to SLEEP mode. This function is enabled independently for each regulator by means of the SLEEP_CTRL1 register bits. Note that the voltage steps are usable with VMODE conversion only. See Appendix A for description of the Digital Scaling Implementation.

Figure 10−4 and Figure 10−5 show the voltage scaling up and voltage scaling down.

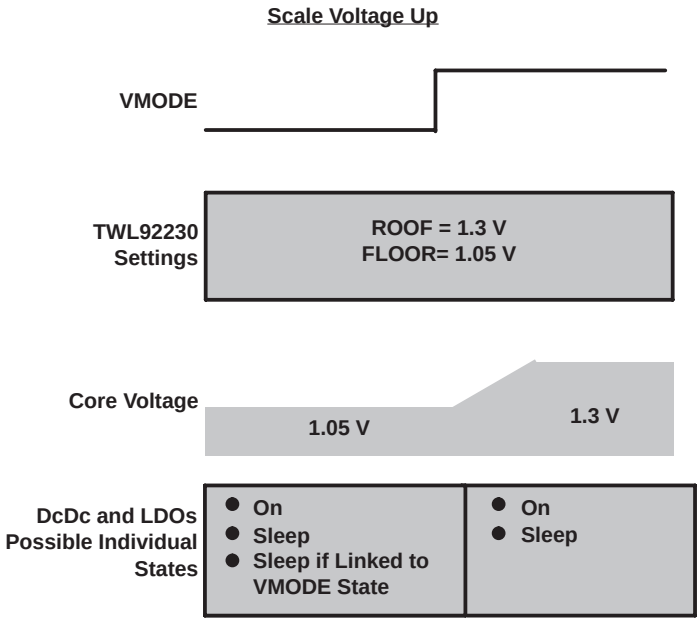


Figure 10−4. VMODE Voltage Scaling Up

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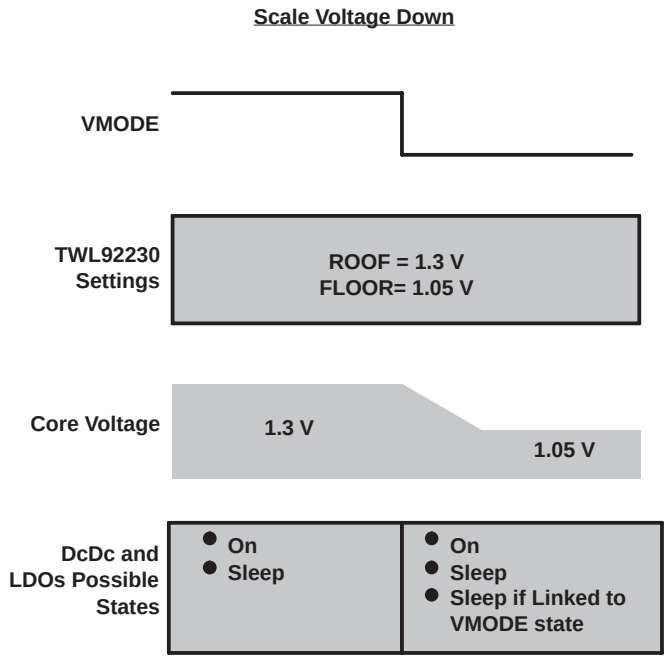


Figure 10−5. VMODE Voltage Scaling Down

10.2 Host Control Outputs

10.2.1 nRESPWRON

nRESPWRON is the output reset signal delivered to the application processor at power on. This active low signal indicates that the power-on sequence is complete. This signal must be held low for sufficient time to allow relevant Application Processor blocks to be operational. See Table 10−7 for timing information.

10.2.2 INT

The interrupt line (INT) is an output from TWL92230 that is used to warn the application processor (active low assertion) that an unmasked interrupt is pending. The application processor can then query the INT_STATUS1 and INT_STATUS2 registers via I^2C to identify the responsible event. The detected events are maskable with INT_MASK1 and INT_MASK2 registers, and the events are cleared by writing to the INT_ACK1 and INT_ACK2 registers. The exact interrupt policy management is detailed in the programming model section.

10.2.3 PWROK

During a power-up sequence, this active high signal indicates that all required regulators are powered up. In addition, during the normal operation, when HW_nSW=1, PWROK is asserted low during a voltage transition on VCORE.

10.3 General-Purpose I/O Port

These three input/output ports can be used for general interface signals.

Alternatively, GPIO2 and GPIO3 can be configured as SLOT_SEL and nSLEEP , respectively.

10.3.1 GPIO1

The GPIO1 becomes an input or output (according to the GPIO_DIR(1) bit in the GPIO_CTRL register. This terminal can be left open if the GPIO_DIR(1) bit is set to 0 (GPIO1 is configured as an output).

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10.3.2 GPIO2 Alternate Function—SLOT_SEL

When the SLOTSELEN bit in the GPIO_CTRL register is set to 1, then GPIO2 becomes an input (SLOT_SEL) and assumes the function of MCT slot selection. When SLOT_SEL=0, SLOT1 is selected. When SLOT_SEL=1, SLOT2 is selected. This function requires SLOT1_EN=SLOT2_EN=1.

When the SLOTSELEN bit in the GPIO_CTRL register is set to 0, then GPIO2 becomes an input or output (according to the GPIO_DIR(2) bit in the GPIO_CTRL register. This terminal can be left open if SLOTSELEN bit is set to 0, and the GPIO_DIR(2) bit is set to 0 (GPIO2 is configured as an output).

10.3.3 GPIO3 Alternate Functions—nSLEEP

When the SLPCTLEN bit in the GPIO_CTRL register is set to 1, then GPIO3 becomes an input (nSLEEP) and assumes the function of sleep control for the regulators. The control of each regulator must be configured with the SLEEP_CTRL2 register. When nSLEEP=1, all regulators configured for sleep control by means of nSLEEP remain in the mode they were in. When nSLEEP=0, all regulators configured for sleep control by means of nSLEEP and that were in the ON mode before the assertion of nSLEEP transition to SLEEP mode.

When the SLPCTLEN bit in the GPIO_CTRL register is set to 0, then GPIO3 becomes an input or output (according to the GPIO_DIR(3) bit in the GPIO_CTRL register. This terminal can be left open if SLPCTLEN bit is set to 0, and the GPIO_DIR(3) bit is set to 0 (GPIO3 is configured as an output).

GPIO3/nSLEEP: see section 10.15, *Sleep Strategy Management*.

10.4 Startup Modes

TWL92230 can start in different configuration modes. The modes are selected by connecting BOOT0 or BOOT1 pins to either LOW (ground) or HIGH (UPR). If the BAKB is not used, these pins can be directly tied to VBAT, but it is recommended that they be tied to UPR. These modes are shown in Table 10−1, where 0 indicates a ground connection and 1 indicates a connection to UPR.

Table 10−1. Startup Modes

BOOT1	BOOT0	CONFIGURATION
0	0	M_Config0
0	1	M_Config1
1	0	M_Config2
1	1	M_Config3

Table 10−2. M_Config0 Description

M_Config0	
ONOFF pin mode	Default mode 1 = TWL92230 ON 0 = TWL92230 OFF
Power-on OMAP IOs	VIO
Power-on OMAP Memories	VMEM
UVLO	Enabled

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The VIO and VMEM LDOs are enabled at startup to power respectively OMAP I/Os and memories for the application processor.

In this configuration IO_1P8 terminal must be tied to VIO terminal (VIO LDO output).

Table 10−3. M_Config1 Description

M_Config1	
ONOFF pin mode	Push button First push: TWL92230 ON Second push: Interrupt generated
Power-on OMAP IOs	VIO
Power-on OMAP Memories	VMEM
UVLO	Enabled

ONOFF input accept a Push Button (see push button function description).

The VIO and VMEM LDOs are enabled at startup to power the OMAP I/Os and OMAP memories, respectively.

In this configuration, IO_1P8 terminal must be tied to VIO terminal (VIO LDO output).

Table 10−4. M_Config2 Description

M_Config2	
ONOFF pin mode	Default mode 1 = TWL92230 ON 0 = TWL92230 OFF
Power-on OMAP IOs	VIO
Power-on OMAP Memories	VMEM
UVLO	Falling edge is disabled

LDOs VIO and VMEM are enabled at startup to power respectively OMAP I/Os and OMAP memories.

NOTE: When TWL92230 is in an application where there is already a battery manager with a UVLO, to avoid unpredictable system behavior, it is chosen to let the master handle the battery UVLO and disable TWL92230 UVLO shutdown functionality.

In this configuration IO_1P8 terminal must be tied to VIO terminal (VIO LDO output).

Table 10−5. M_Config3 Description

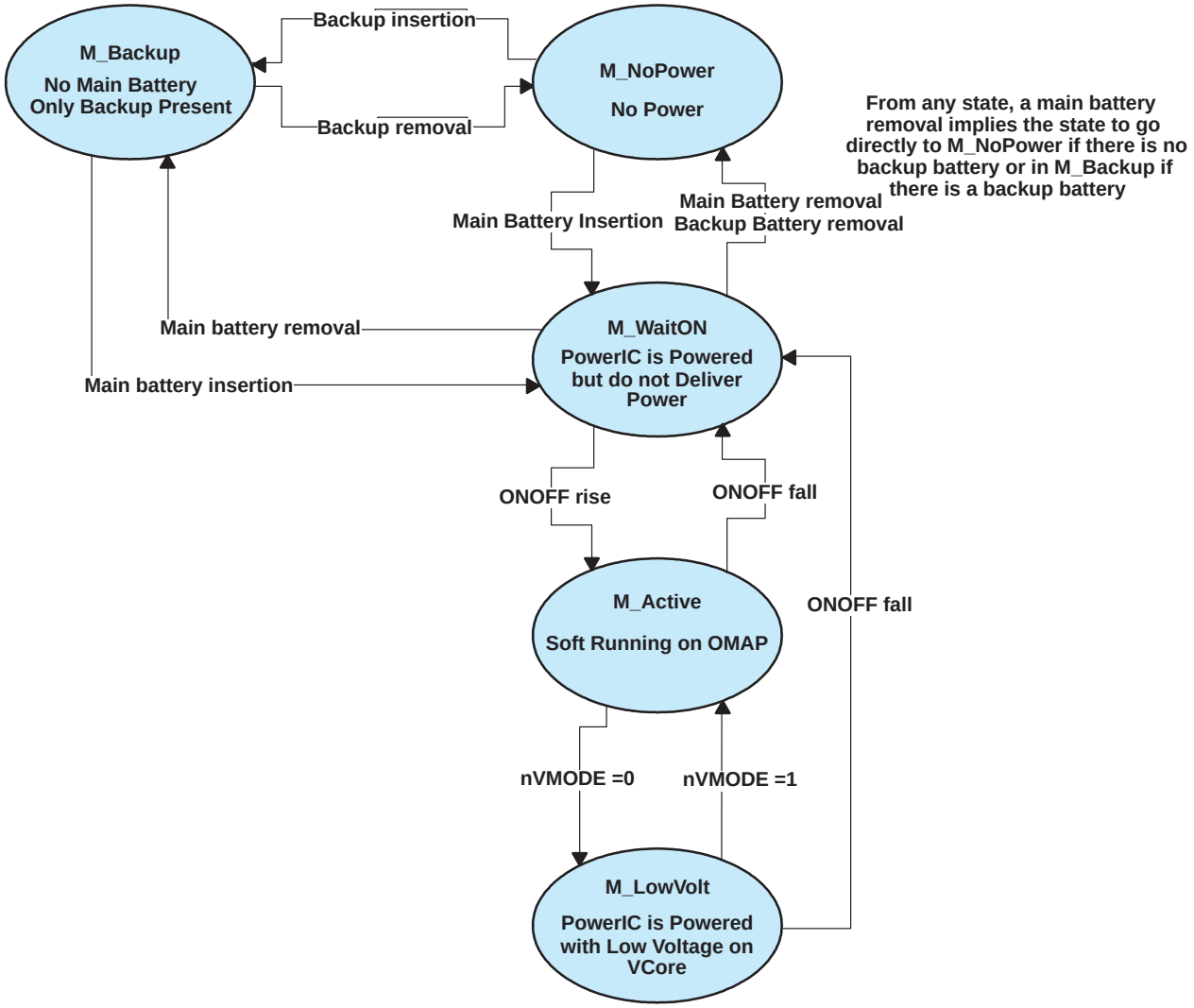
M_Config3	
ONOFF pin mode	Default mode 1 = TWL92230 ON 0 = TWL92230 OFF
Power-on OMAP IOs	DCDC2
Power-on OMAP Memories	DCDC2
UVLO	Versions prior to PG2.2 Enabled or disabled accordingly to UVLO_BYP bit in the DETECT_CTRL register. PG2.2 and later versions Enabled or disabled accordingly to UVLO_EN bit in the DETECT_CTRL register. Falling edge is disabled by default at startup. Once the device has startup, this register can be changed by writing to the DETECT_CTRL register.

LDOs VIO and VMEM are disabled at startup. DCDC2 is enabled at startup at 1.8 V to power both OMAP I/Os and OMAP memories. In this configuration, IO_1P8 must be tied to DCDC2.VOUT (DCDC2 buck converter output). The goal of this configuration is to avoid using the I/Os and memory LDOs to reduce the power dissipation or, in other words, gain efficiency. The risk is noise propagation between OMAP I/Os and memories.

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10.5 State Machine Without Pushbutton (Default Mode)

In this case ONOFF signal is the only way to move M_WaitON to/from M_Active and M_LowVolt to M_WaitOn



M_Active : PowerIC is powered and Full power is available (DC/DC and LDOs)

M_LowVolt : PowerIC is powered delivers low voltage on VCore

M_WaitON : PowerIC is powered but do not deliver power

M_Backup : Only backup battery is present

M_NoPower : PowerIC is not powered

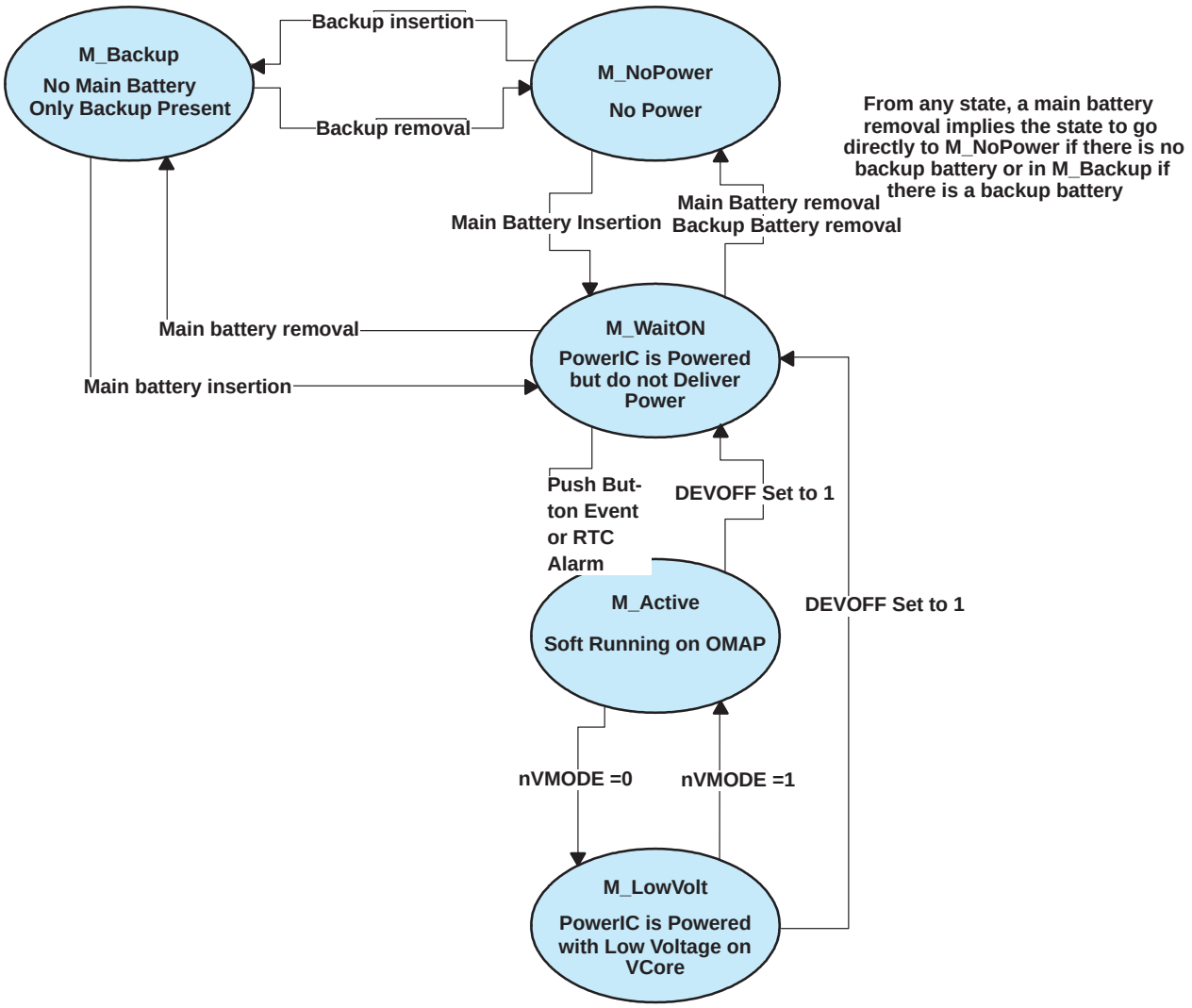
Figure 10−6. State Machine Without Pushbutton (Default Mode)

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10.6 State Machine with Pushbutton

An action on the pushbutton or an RTC alarm event can turn TWL92230 from M_WaitON to M_Active.

When in M_Active, a pushbutton on TWL92230 will raise an interrupt from TWL92230 to OMAP. OMAP then detects that the interrupt was a pushbutton event. OMAP then can take the decision to shutdown by setting the DEVOFF bit in TWL92230 to 1. When in M_LowVolt, a pushbutton on TWL92230 will raise an interrupt from TWL92230 to OMAP. OMAP then detects that the interrupt was a pushbutton event. OMAP then can take the decision to shutdown by setting the DEVOFF bit in TWL92230 to 1.



M_Active : PowerIC is powered and Full power is available (DC/DC and LDOs)

M_LowVolt : PowerIC is powered delivers low voltage on VCore

M_WaitON : PowerIC is powered but do not deliver power

M_Backup : Only backup battery is present

M_NoPower : PowerIC is not powered

Figure 10−7. TWL92230 State Machine with Pushbutton

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10.7 System Power State

Table 10−6. TWL92230 System States

SYSTEM STATE	COMMENTS	VBAT CURRENT
M_NoPower	No activity in TWL92230	0 µA
M_Backup	TWL92230 is powered by the backup battery. Only essential circuitry is working: • 32-kHz oscillator • RTC • VDIG LDO • BBSMS This maintains the date in the RTC.	< 20 µA
M_WaitOn	TWL92230 is powered by the main battery. Besides essential circuitry (above) the following circuitry is working: REFSYS	< 70 µA
M_Active	TWL92230 is powered by the main battery. The main battery has sufficient voltage to allow the system to start At least the following resources are on: CLKGEN VCORE converter DCDC2 converter VPLL VIO (depending on the configuration) VMEM (depending on the configuration) All resources are available	Limit of the package dissipation
M_LowVolt	TWL92230 is powered by the main battery, but VCORE is at low voltage. All resources can be used. This state can modify VCORE voltage level.	Depending on the application

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10.8 From M_NoPower to M_WaitON to M_Active (Startup)

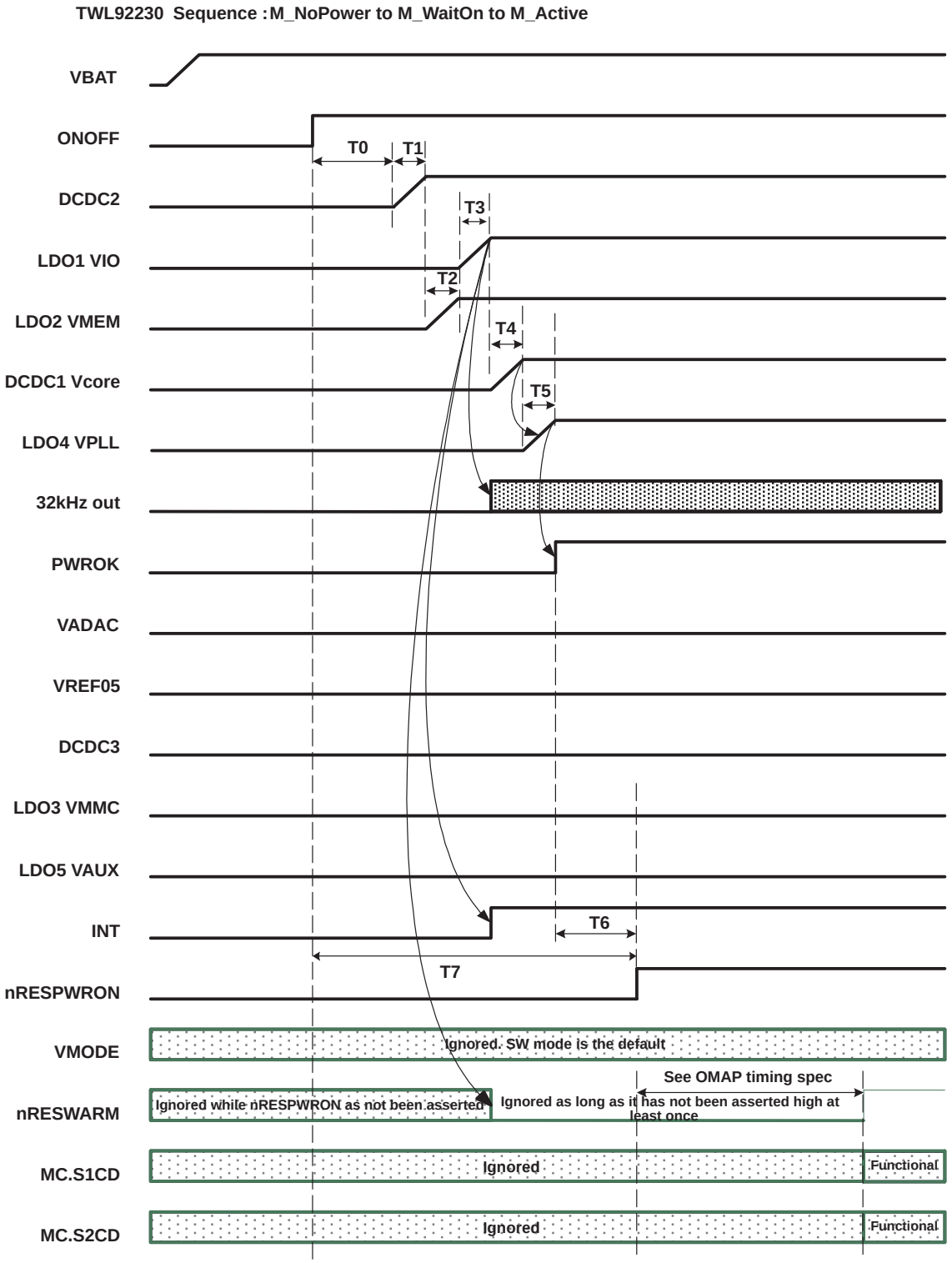


Figure 10−8. M_NoPower to M_WaitON to M_Active

PRODUCT PREVIEW

When the battery voltage is present, the V_{REF} and VDIG are immediately started and set.

The 32-kHz oscillator starts if a crystal is present on its pins.

The application or user can then request the powerup of OMAP by setting the ONOFF signal.

This action starts all the resources to boot OMAP device following the required sequence:

1. After ONOFF signal is asserted high, it takes T0 to TWL92230 to start the power-up sequence.
2. DCDC2 starts first as it is used to supply power to LDO1-VIO, LDO2-VMEM
3. Once DCDC2 has completed its ramp-up, then LDO2-VMEM is enabled.
4. Once LDO2-VMEM has completed its sequence, LDO1-VIO starts ramping up.
5. When LDO1-VIO has completed its power up, OMAP I/Os are powered. Now it is possible to apply signals to OMAP I/Os. From TWL92230, the 32-kHz output as well as the INT signals are applied to OMAP.
6. When LDO1-VIO has completed its power-on sequence, the DCDC1-VCORE is enabled and starts its ramp up sequence.
7. When VCORE DCDC1 ramp up is complete, LDO4_VPLL starts ramping up.
8. When LD04-VPLL has ramped up, the PWROK signal is asserted to signal that the OMAP24xx power-up sequence has been completed.
9. A timer starts and waits 8 ms (T6) to ensure that the OMAP24xx high speed clock is stabilized.
10. After 8 ms (T6), the nRESPWRON signal is asserted high by TWL92230 (see Figure 10−9 and Figure 10−10 for nRESPWRON being gated by 32-kHz duty-cycle detection feature).
11. OMAP24xx will release nRESWARM (High state). This signal is an input to TWL92230, please see OMAP specification for timing detail).

The timing diagrams in this section will use the timings described in Table 10−7. Note these timings were derived from digital control block which used 600-kHz internal clock generator. See actual regulator turn on/off times.

Table 10−7. Power Transition Timings

PARAMETER	TIMING	MIN	TYP	MAX	UNIT
ONOFF high to DCDC2 startup	T0(1)	23	650	975	µs
DCDC2 on time	T1	545	600	667	µs
VMEM on time	T2	194	213	237	µs
VIO on time	T3	194	213	237	µs
DCDC1 on time	T4	545	600	667	µs
VPLL on time	T5	194	213	237	µs
VPLL to nRESPWRON	T6	8	8.80	9.78	ms
ONOFF to nRESPWRON	T7	9.7	11.25	12.8	ms

(1) T0 is measured at VBAT of 2.4 V with a slew of 1 ms from 0 to 3.6 V. The TYP and MAX timings are measured with ONOFF tied with VBAT. Note the delay will decrease (~50 µs typical) if VBAT is applied long before ONOFF is asserted.

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10.9 From M_Active to M_WaitON (DEVOFF) (Shutdown DEVOFF)

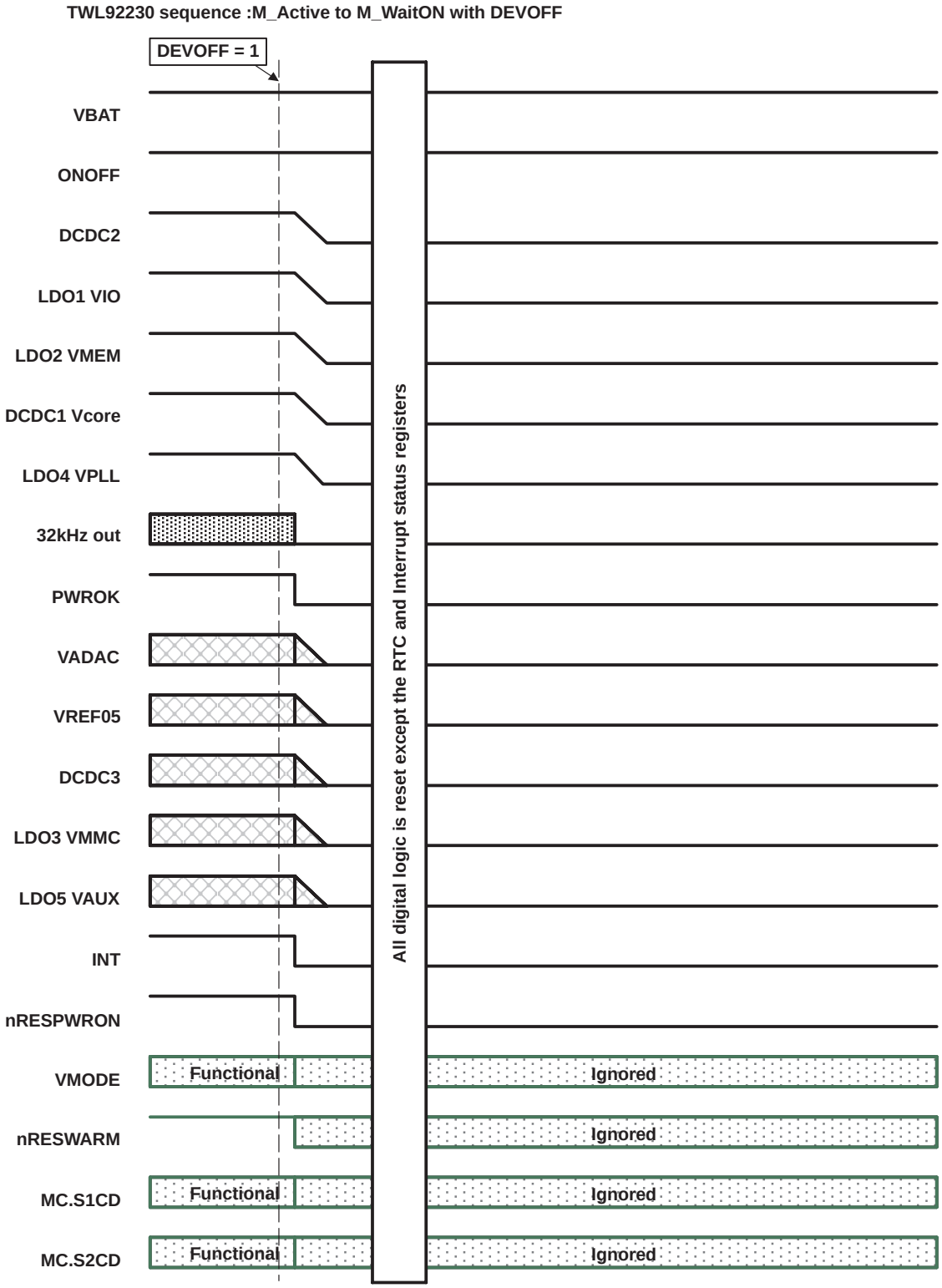


Figure 10−9. From M_Active to M_WaitON (DEVOFF)

PRODUCT PREVIEW

It is possible to shutdown TWL92230 via software, using the DEVOFF bit.

When setting this bit, the following sequence occurs:

1. All dc-dc converters and LDOs are shutdown at the same time. Also, the TWL92230 I/Os (32-kHz_out, PWROK, INT, and nRESPWRON) are turned off at the same time.
2. All digital logic is reset except the RTC and Interrupt status registers.

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10.10 From M_Active to M_WaitON (ONOFF) (Shutdown ONOFF)

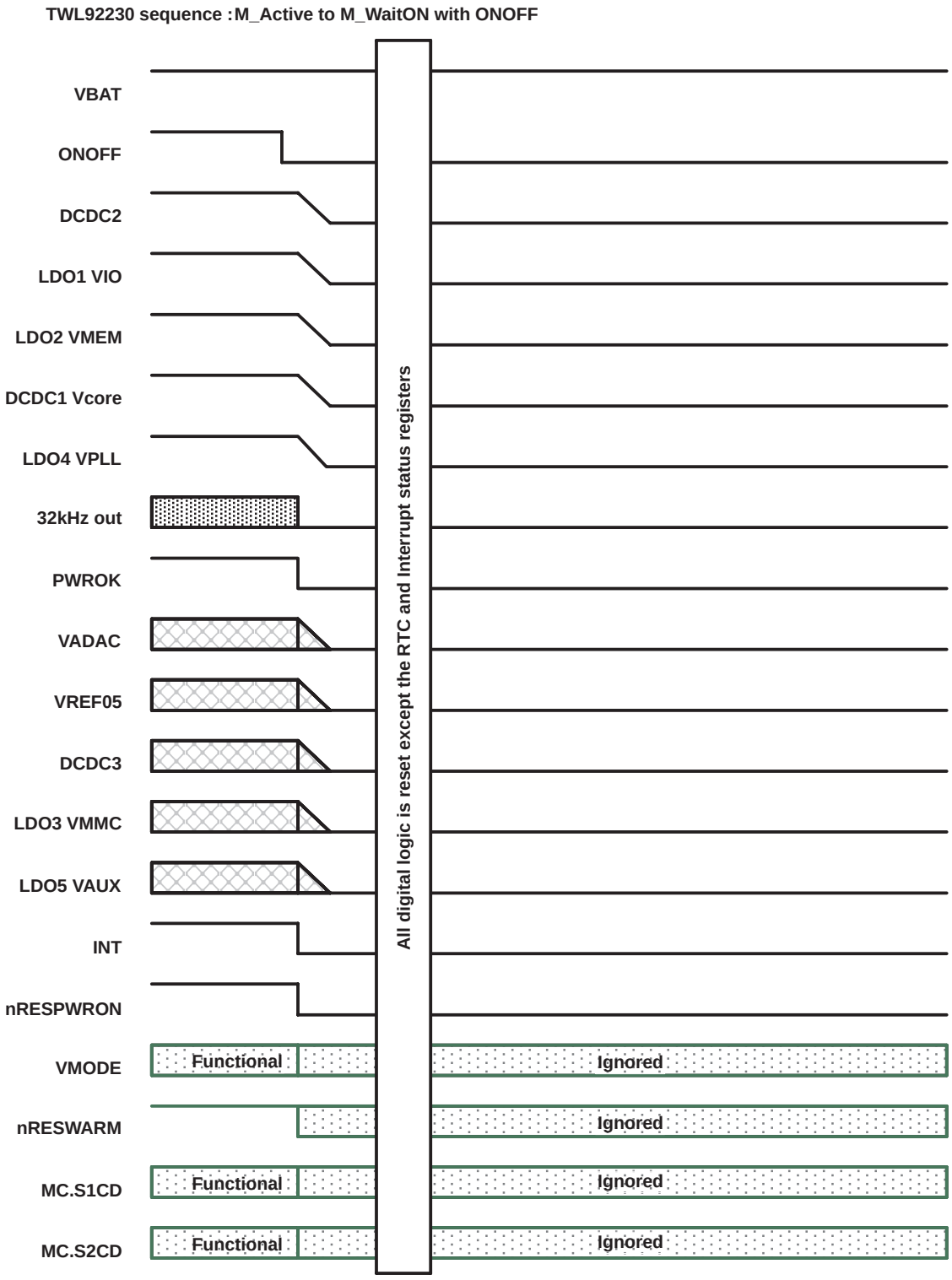


Figure 10−10. From M_Active to M_WaitON (ONOFF)

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1. ONOFF signal is asserted low
2. All dc-dc converters and LDOs are shutdown at the same time. Also, the TWL92230 I/Os (32-kHz_out, PWROK, INT, and nRESPWRON) are turned off at the same time.
3. All digital logic is reset except the RTC and the boot mode is sampled at startup

10.11 From M_WaitON to M_Active (Wakeup)

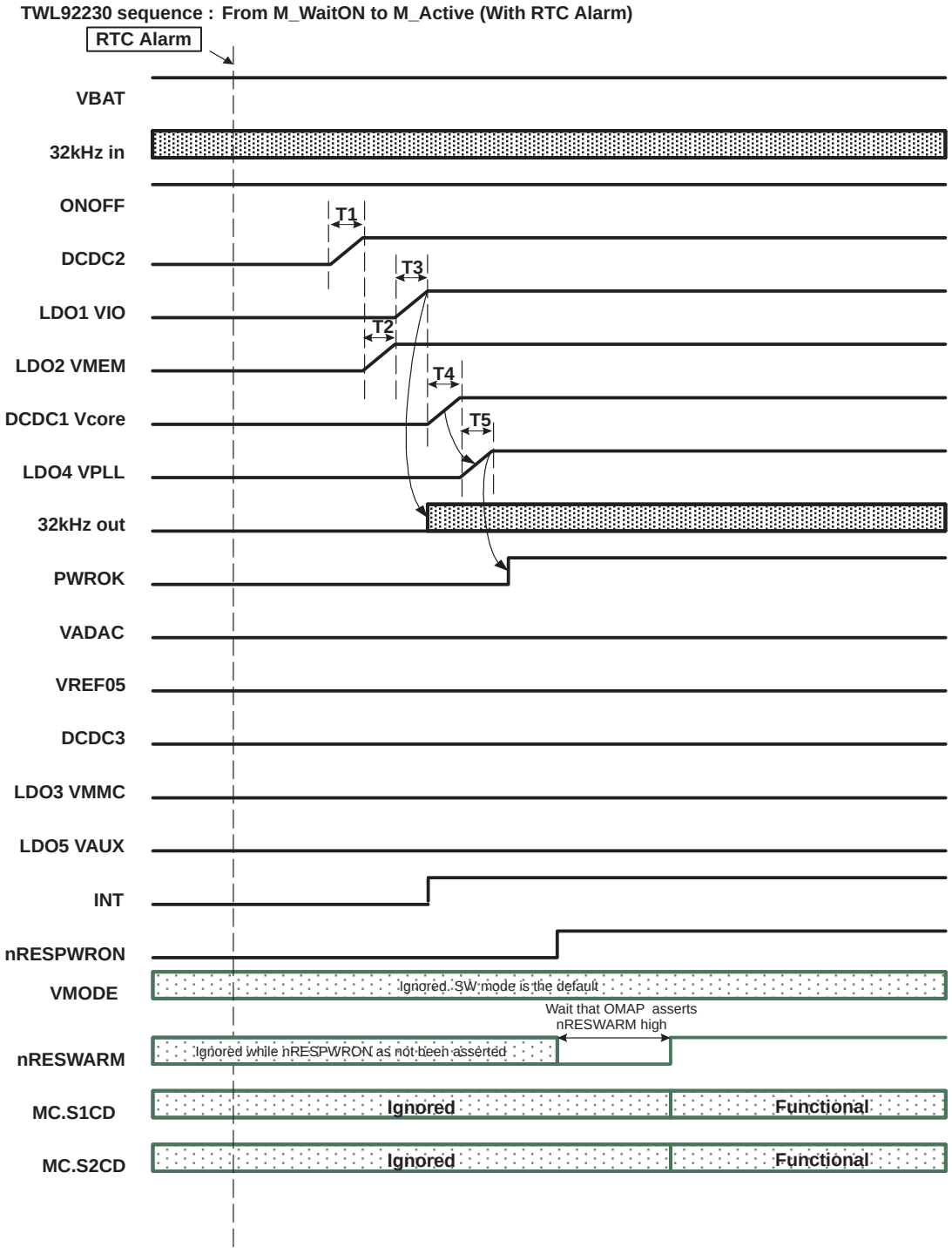


Figure 10−11. From M_WaitON to M_Active

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Upon the detection of an RTC alarm, TWL92230 starts a wake-up sequence.

DCDC2 starts first as it is used to supply power to LDO1-VIO, LDO2-VMEM.

1. Once DCDC2 has completed its ramp-up, then LDO2-VMEM is enabled.
2. After LDO2-VMEM is enabled, LDO1-VIO starts ramping up.
3. When LDO1-VIO has complete its power up, OMAP I/Os are powered. Now it is possible to apply signals to OMAP I/Os. From TWL92230, the 32-kHz output is applied to OMAP.
4. When LDO1-VIO has completed its power-on sequence, the DCDC1-VCORE is enabled and starts its ramp-up sequence.
5. When DCDC1-VCORE is complete, LDO4-VPLL starts ramping up.
6. When LD04-VPLL has ramped up, the signal PWROK is asserted to signal that the OMAP24xx power-up sequence has been completed.
7. A timer starts and waits 8 ms (T6) to ensure that the OMAP24xx high speed clock is stabilized.
8. After 8 ms (T6), the nRESPWRON signal is asserted high by TWL92230 (see chapter 10.17 for nRESPWRON being gated by 32-kHz duty-cycle detection feature).
9. OMAP24xx will release nRESWARM (High state). This signal is an input to TWL92230, please see OMAP specification for timing detail).
10. INT signal will not be asserted low by TWL92230 due to the RTC alarm because the MASK bits have been set to their default values. However, the RTC alarm interrupt status bit will remain set and will cause the external INT pin to go low once the corresponding MASK bit is cleared.

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10.12 From M_Active to M_LowVolt to M_Active (LowVolt)

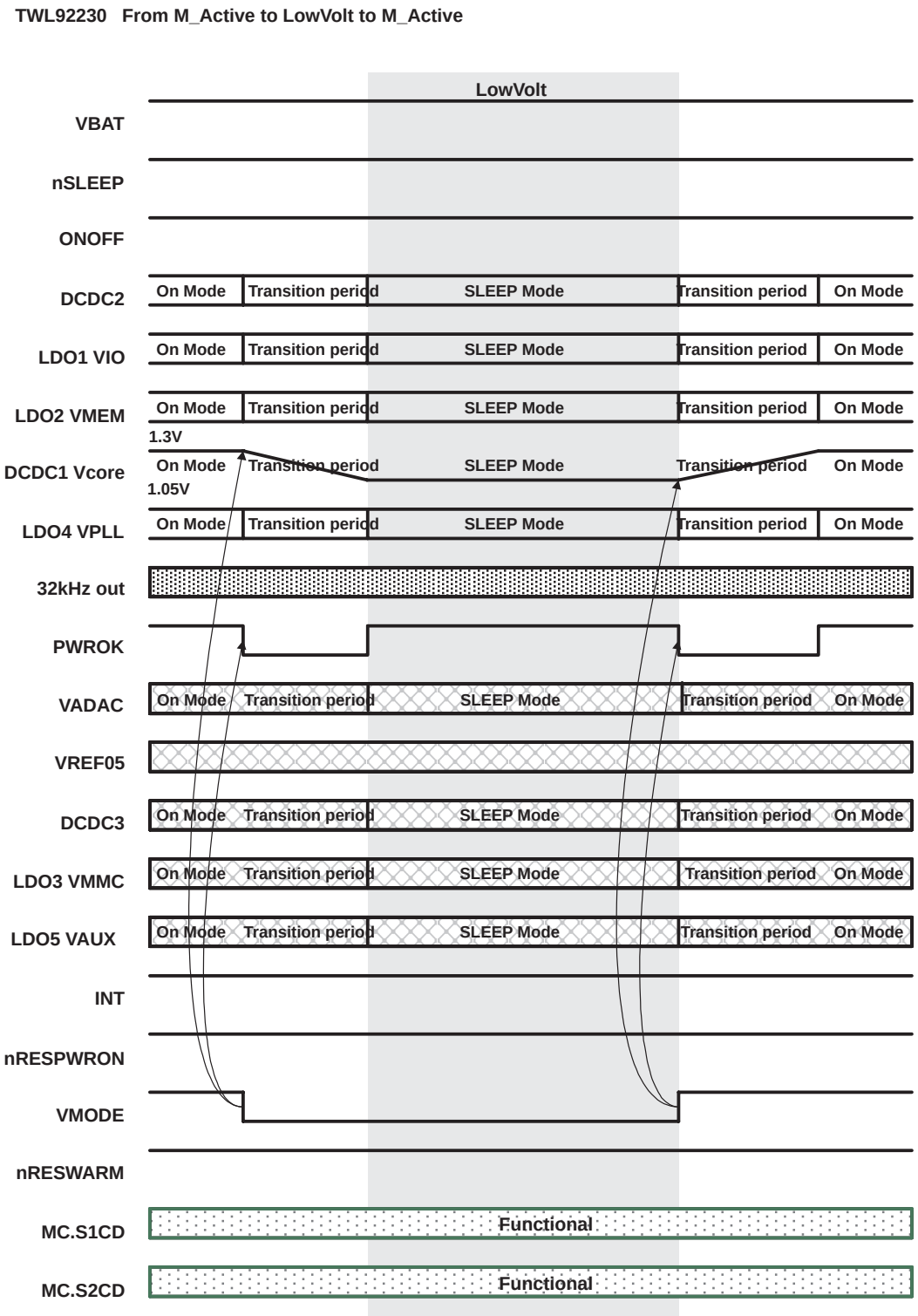


Figure 10−12. From M_Active to M_LowVolt to M_Active

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10.12.1 From M_Active to M_LowVolt

The low voltage sequence is initiated when OMAP24xx asserts the VMODE signal to low.

Upon the reception of the VMODE signal, TWL92230 starts entering the low voltage mode:

1. PWROK signal goes low. At the same time DCDC1_VCORE decreases its voltage to the FLOOR voltage.
2. At the same time, all LDOs and dc-dc converters that have their xxxSLPEN1 bit set will start their transition sequence from the On mode to sleep mode. LDOs and dc-dc converters that don't have their xxxSLPEN1 bit set will remain in the On mode (see SLEEP_CTRL1 register description).
3. Once DCDC1_VCORE has reached the FLOOR voltage, the signal PWROK signal is asserted high to inform OMAP24xx that the low voltage sequence is completed.

10.12.2 From M_LowVolt to M_Active

OMAP24xx can decide to exit the M_LowVolt mode by asserting the VMODE signal high.

1. VMODE is asserted high.
2. TWL92230 initiates the sequence by setting the PWROK signal low, and starts ramping up DCDC_VCORE voltage to the ROOF value.
3. All LDOs and dc-dc converters that were in sleep mode as a consequence of their xxxSLPEN1 bit setting and the VMODE signal, start transitioning to On mode.
4. When the ROOF value is reached, the PWROK signal is asserted high to inform OMAP24xx that the transition from M_LowVolt to M_Active is complete.

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10.13 From M_NoPower to M_WaitON to M_Active (M_Config3) (Startup)

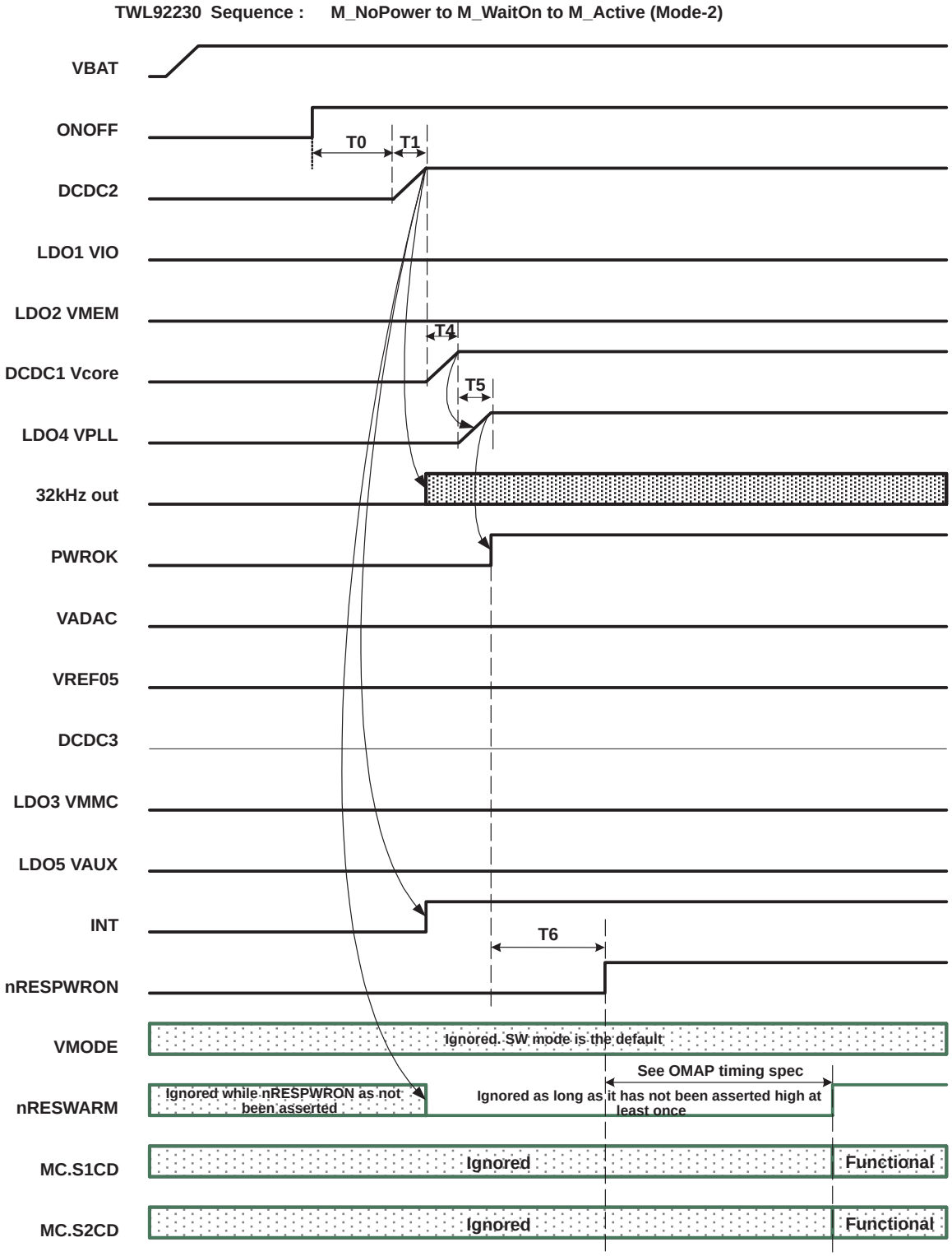


Figure 10−13. M_NoPower to M_WaitON to M_Active (M_Config3)

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When battery is not present, and no backup battery is inserted, the system is in M_NoPower state.

When the battery voltage is present, the VREF and VDIG are immediately started and set.

There are 2 ways to generate 32-kHz clock to the RTC and 32KOUT within the TWL92230. A 32-kHz oscillator starts if a crystal is present on its pins (XIN and XOUT), or a digital 32-kHz clock is applied on the XIN ball. See chapter 6.1 for details.

The application or user can request the powerup of OMAP by setting the ONOFF signal.

This action starts all the resources to boot OMAP device following the required sequence:

1. After ONOFF signal is asserted high, it takes T0 to TWL92230 to start the power-up sequence.
2. DCDC2 starts first and is used to power OMAP I/Os, memory I/Os, and memory cores.
3. Now it is possible to apply signals to OMAP I/Os. From TWL92230, the 32-kHz output and the INT signals are applied to OMAP
4. The DCDC_VCORE is enabled and starts its ramp up sequence.
5. When VCORE DCDC1 ramp up is complete, LDO4_VPLL starts ramping up.
6. When LD04_VPLL has ramped up, the PWROK signal is asserted to signal that the OMAP24xx power-up sequence has been completed.
7. A timer starts and waits 8 ms (T6) to ensure that the OMAP24xx high speed clock is stabilized.
8. After 8 ms (T6), the nRESPWRON signal is asserted high by TWL92230 (see chapter 10.17 for nRESPWRON being gated by 32-kHz duty-cycle detection feature).
9. OMAP24xx will release nRESWARM (High state). This signal is an input to TWL92230, please see OMAP specification for timing detail).

10.14 Voltage Scaling Management

In order to reduce the power consumption of the application processor, TWL92230 can scale the VCORE voltage. There are two different strategies: by software or by hardware and it can be selected by the the HW_nSW bit:

More information of the control and value bits mentioned below is shown in the VCORE register in section 11.2, *Register Map*.

- Direct Scaling Software Strategy:

  The application processor writes the VCORE voltage needed directly to the VCORE_VOLT via the I^2C. The VCORE_VOLT bits are connected to the VCORE buck converter and therefore the voltage change for the software strategy occurs immediately. In this mode, the PWROK signal is not used.

- Synchronized Scaling Hardware Strategy:

  The application processor programs via I^2C the VCORE voltages associated with the two states of VMODE signal: the roof and the floor values. The application processor also writes the STEP_PER value that is used if multiple-step mode is used (see below). TWL92230 state machine updates the VCORE_VOLT settings every time the signal VMODE changes and also for each step change for the multiple-step mode (see below). In this mode, the PWROK signal goes low for the duration of the transition and returns high once the transition has completed.

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Two voltage scaling modes are available for the synchronized scaling strategy, The multiple-step mode and the single-step mode, that are selected by the STEP_nJMP bit:

- Voltage Scaling Multiple-Step Mode:

  In multiple-step mode, TWL92230 scales the VCORE voltage by steps of 25 mV between the roof and floor values. The transition time between each step is provided by the STEP_PER value and it is a multiple of 10 µs.

- Voltage Scaling Single-Step Mode:

  In single-step mode, TWL92230 switches the VCORE voltage directly between the roof and floor values, without controlling the ramp time or having intermediate step.

See Appendix A for detailed information on the voltage scaling implementation.

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10.15 Sleep Strategy Management

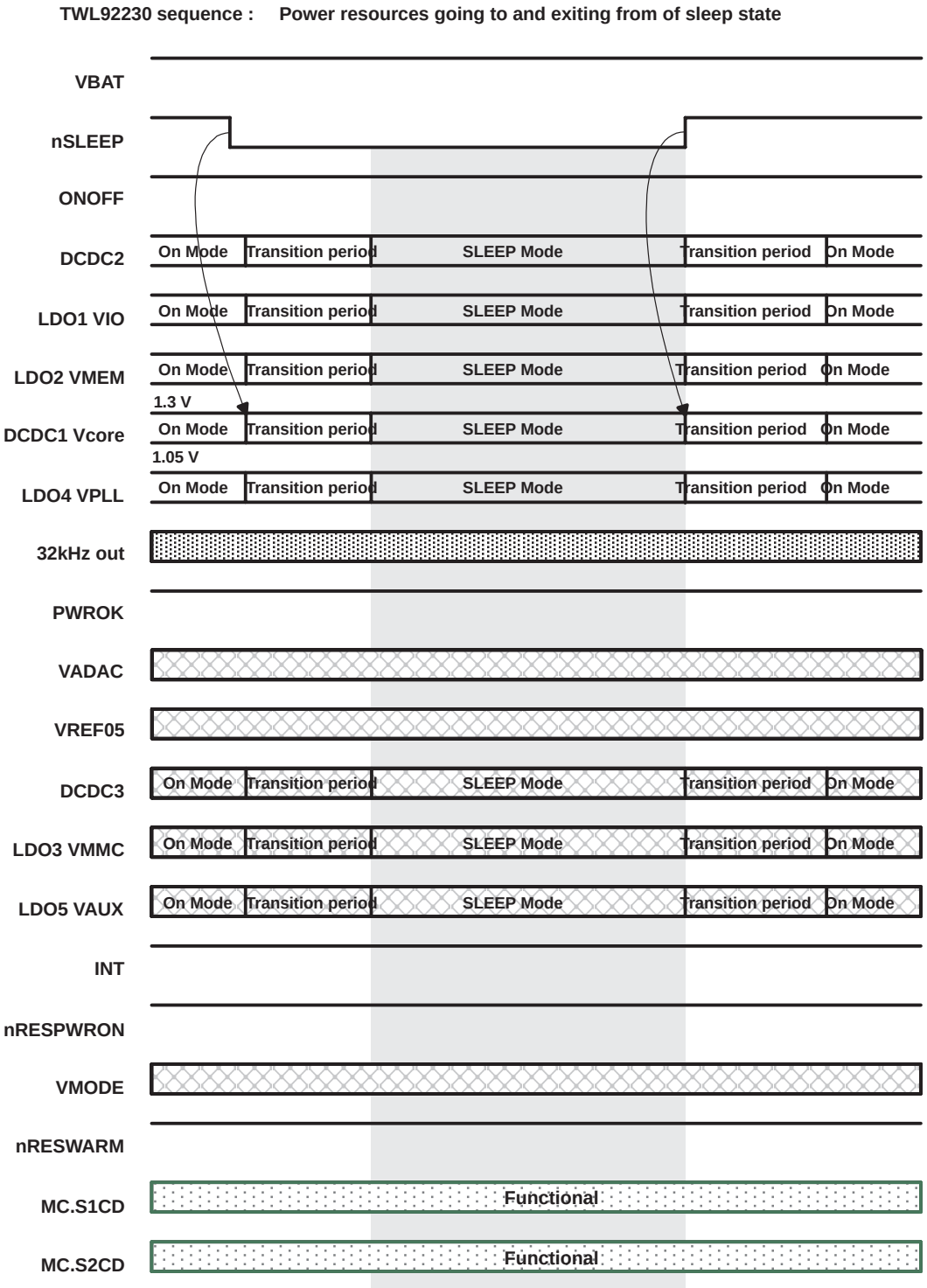


Figure 10−14. Sleep Transition During The M_Active State

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10.15.1 Transition from On Mode to Sleep Mode

The transition from the On mode to sleep mode is initiated when OMAP24xx asserts the signal nSLEEP (sys.clkreq) to low.

Upon the reception of the nSLEEP signal low, TWL92230 starts entering the sleep mode: All concerned LDOs and dc-dc converters (that is, those that have their xxxSLPEN2 bit set to 1) are transitioning to their sleep mode.

10.15.2 Transition from Sleep Mode to On Mode

OMAP24xx can decide to exit the sleep mode by asserting the nSLEEP (sys.clkreq) signal high. The sequence is as follows:

1. nSLEEP is asserted high.
2. TWL92230 releases all concerned LDOs and dc-dc converters from their sleep mode to their On mode.

10.16 Hardware Sleep Implementation

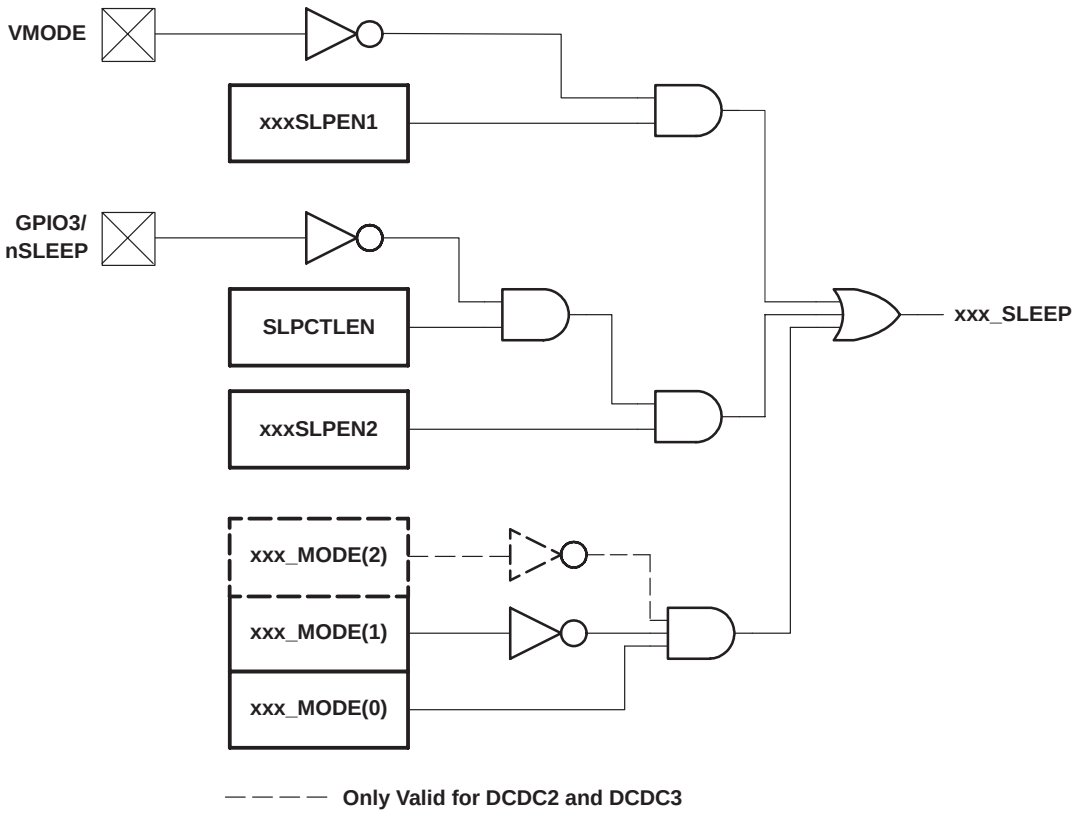


Figure 10−15. Hardware Sleep Implementation

Each regulator can be put into sleep mode by one of three ways:

- By directly writing to the I^2C bits corresponding to the mode for that regulator, xxx_MODE
- By means of the VMODE pin (requires configuration of the SLEEP_CTRL1 register)
- By means of the GPIO3/nSLEEP pin (requires configuration of the SLEEP_CTRL2 register and enabling the alternate function for GPIO3 by setting the SLPCTLEN bit in the GPIO_CTRL register)

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If the regulator is disabled by means of the xxx_MODE bits, the regulator remains disabled regardless of the configuration of the SLPCTLEN, xxxSLPEN2, and xxxSLPEN1, or the state of the VMODE and GPIO3/nSLEEP pins.

This method of control allows VMODE or GPIO3/nSLEEP to independently force any of the regulators from the ON mode to the sleep mode of operation.

10.17 32-kHz Duty Cycle Detection

The TWL92230 power-up state machine does not require the 32-kHz clock to be present in order for it to operate since it operates from the internal 600-kHz clock. The startup time of the clock generator that generates the 600-kHz clock is much faster than the startup time of the 32-kHz oscillator. Therefore, it is possible that the power-up state machine is ready to deassert the nRESPWRON signal before the 32-kHz clock is available on the 32KOUT pin. For example, if BKBAT and VBAT are applied to the respective terminals of the TWL92230 at the same time, and the ONOFF pin (in M_Config0, M_Config2 and M_Config3) is asserted shortly after, the power-up state machine may be ready before the 32K oscillator has had time to start and stabilize. A duty cycle detection circuit can be enabled by means of the 32KDETEN pin, which will use the 600-kHz clock to measure the duty cycle (not absolute frequency) of the 32-kHz clock coming from the oscillator block. See Figure 10−16 (which is a portion of Figure 6−1) for 32-kHz duty cycle detection and nRESPWRON gating.

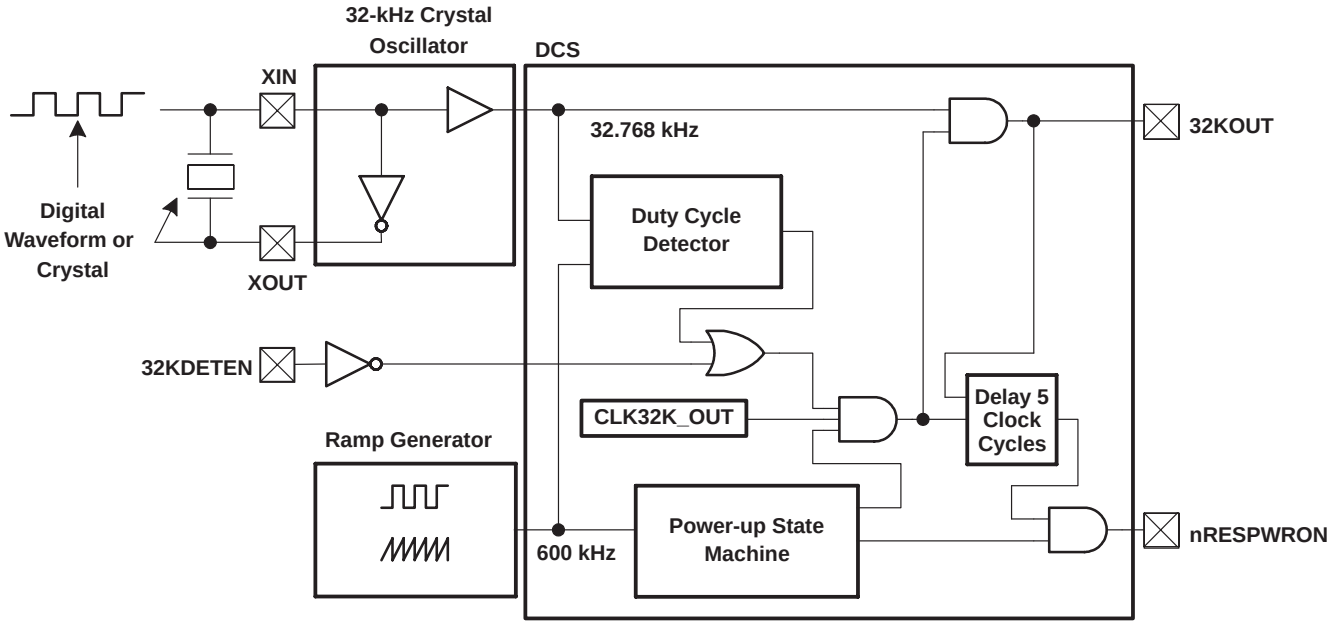


Figure 10−16. nRESPWRON Gating

If the duty cycle detector circuit senses that the 32K clock signal meets a minimum duty cycle criteria, then the power-up state machine's nRESPWRON signal is allowed to pass through as long as at least five 32-kHz clock cycles have been seen on the 32KOUT pin. If the duty cycle does not meet the minimum criteria, then the internal nRESPWRON signal is gated until the minimum criteria is met and at least five 32-kHz clock cycles have been seen on the 32KOUT pin. It is important to note that the duty cycle detection is a "one shot" circuit; that is, it is only reset when both VBAT and BKBAT have fallen below the minimum respective thresholds, causing an internal power-on-reset (POR) event. Once the duty cycle detector circuit fires, it is shut down to save power and will not start again until a POR event. If the 32-kHz clock is ever stopped, but no POR event has reset the duty cycle detector circuit, then any subsequent transitions into the M_Active state will not gate the nRESPWRON signal due to the lack of a 32-kHz clock.

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The criterion for the duty cycle of the clock coming from the 32-kHz oscillator block is that a minimum 32-kHz clock high time be followed by a minimum 32-kHz clock low time for 16 consecutive clock cycles. If one of those 32-kHz clock high times or clock low times is less than the minimum, then the detection circuit starts over looking for the first minimum 32-kHz clock high time. It is important to note that if we consider the duty cycle of a waveform to be the measure of the portion of the clock cycle that the clock signal is high, then the minimum criteria could be the measure of a maximum duty cycle based on the way the duty cycle detector looks at the high and low times of the clock signal as being equally important parameters. The clock high times and clock low times are measured with respect to the internal 600-kHz clock. Assuming a ±10% variation of the internal 600-kHz clock, the following minimum clock-low-times and clock-high-times make up the minimum criteria.

Table 10−8. Clock High/Low Times

MINIMUM CRITERION	MIN	TYP	MAX	UNIT
Clock low time	5.89	6.53	7.08	µs
Clock high time	5.89	6.53	7.08	µs

This is to say that if the 600-kHz clock is running 10% fast, a 19.3% to 80.7% duty cycle waveform may be seen on the 32KOUT pin, assuming a 30.517-µs clock period. Conversely, if the 600-kHz clock is running 10% slow, a 23.2% to 76.8% duty cycle waveform may be seen on the 32KOUT pin, assuming a 30.517-µs clock period.

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11 I2C Serial Interface and Register Map

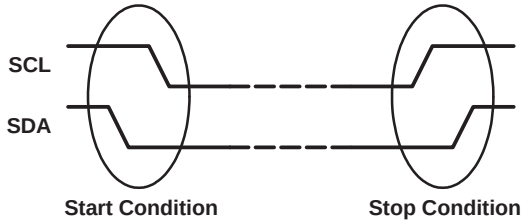
11.1 I2C Serial Interface

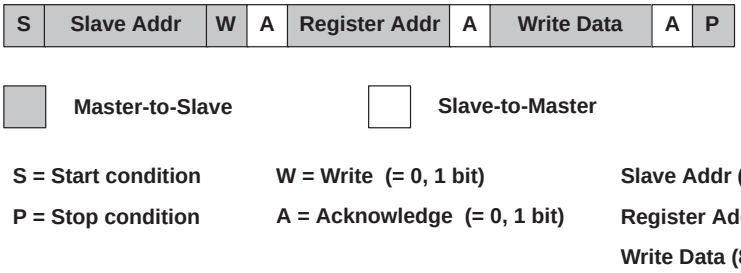
This block allows communication and control between the application processor and TWL92230. It is the means by which the registers within the device are accessed so the modes and parameters in the blocks can be changed. The serial interface is implemented as an I2C bus with two signals: bidirectional data and clock input. A two-byte serial protocol using the format of one byte address and one byte data is used. For detailed information see the *I2C-Bus Specification*.

The standard I2C protocol is implemented but the device operates as a slave only. The master of the bus must be able to perform writes to and reads from registers on the device via the I2C interface. TWL92230 has the fixed slave address of 0x72.

The device monitors the bus for valid slave addresses all the time. The device generates an acknowledge bit if the slave address is true. A start condition is identified by a high-to-low transition of the SDA line while the SCL is stable in the high state. A stop condition is identified by a low-to-high transition of the SDA line while the SCL is stable in the high state. When data is to be written to register(s) in the device, the protocol in Figure 11−1 applies. When data is to be read from a register in the device, the protocol in Figure 11−1 applies and is supported by the device.

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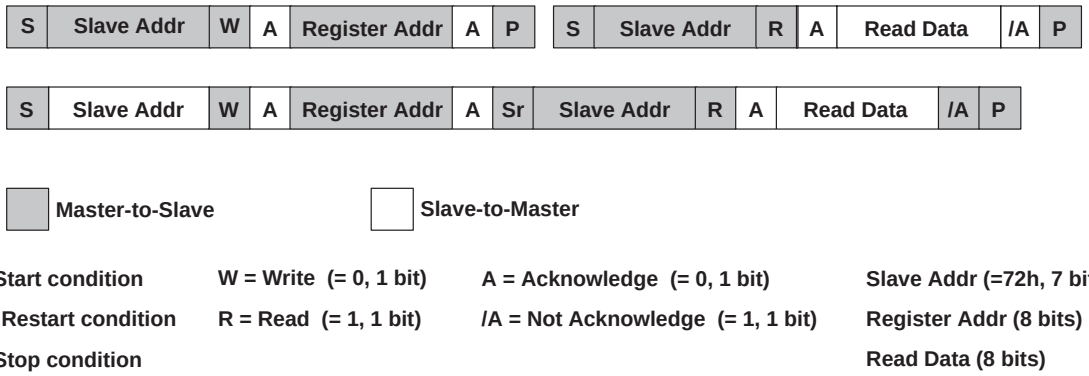


Figure 11−1. I2C Write and Read Protocol Sequence

If a new start or stop condition appear within a message, the bus returns to the idle mode again. The data bytes are transferred with the MSB being transmitted first both during read and write operations.

Bit order:
Address (7:0) = ABCD EFGH, A:MSB and H:LSB.
Data (7:0) = ABCD EFGH, A:MSB and H:LSB.

The MSB is sent first, both in the address word and in the data word.

Consecutive (page) read out is initiated from the master by sending acknowledge instead of not acknowledge after receipt of data. The I2C register bank then increments the address pointer to the next I2C address and sends the data to the master. This procedure is repeated until the master sends a not acknowledge after receipt of data. If a nonexisting I2C address is read out then TWL92230 must return 0s. All test registers must be at the end of the I2C bank in order not to create confusion about which register that was actually read out in page mode.

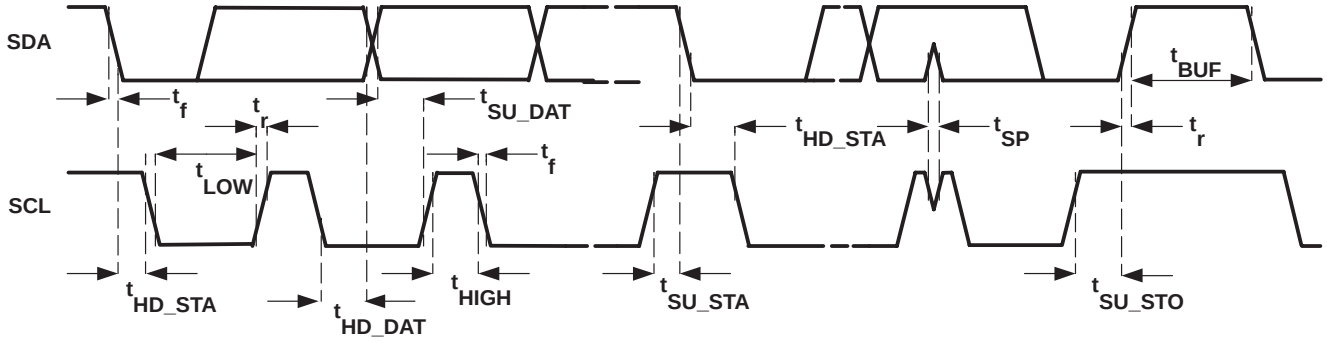


Figure 11−2. Definition of Timing for Fast-Mode Device on the I2C Bus

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The I²C serial interface timing specifications are shown below.

Table 11−1. I²C Serial Interface Timing Specifications

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency (f_{SCL})			400	kHz
t_{HIGH}	High period of the SCL clock (t_{HIGH})	600			ns
t_{LOW}	Low period of the SCL clock (t_{LOW})	1300			ns
t_{HD_STA}	Hold time (repeated) start condition. After this period the first clock pulse is generated (t_{HD_STA})	600			ns
t_{SU_STA}	Setup time for repeated start condition (t_{SU_STA})	600			ns
t_{HD_DAT}	Data input hold time (t_{HD_DAT})	300(1)		900(2)	ns
t_{SU_DAT}	Data input setup time (t_{SU_DAT})	100(3)			ns
t_r	Rise time of both SDA and SCL signals (t_r)	20 + 0.1Cb(4)		300	ns
t_f	Fall time of both SDA and SCL signals (t_f)	20 + 0.1Cb(4)		300	ns
t_{SU_STO}	Setup time for stop condition (t_{SU_STO})	600			ns
t_{BUF}	Bus free time between a stop and a start condition (t_{BUF})	1300			ns
t_{SP}	Pulse width of spikes which must be suppressed by the input filter (t_{SP})			50	ns
Cb	Capacitive load for each bus line (Cb)			400	pF

(1) A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.
(2) The maximum t has only to be met if the device does not stretch the low period (t) of the SCL signal.
(3) A fast mode I²C bus device can be used in a standard I²C bus system, but the requirement t = 250 ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device stretches the low period of the SCL signal, it must output the next data bit to the SDA line t + t = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification) before the SCL line is released.
(4) C_b = total capacitance of one bus line in pF.

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11.2 Register Map

This section contains the description and usage of all 68 8-bit registers of TWL92230 that are accessible by the I2C interface.

11.2.1 Revision Register

Address: 0x01
Reset: 0xXY (X is the major revision and Y is the minor revision. Example: 0x10 for TWL92230 PG 1.0)
Description: Contains binary coded decimal (BCD) information about the revision of the device

	D7	D6	D5	D4	D3	D2	D1	D0
Name	MAJOR_REV(3:0)				MINOR_REV(3:0)			
Read/Write	r	r	r	r	r	r	r	r
Reset Value	X	X	X	X	Y	Y	Y	Y

FIELD NAME	DESCRIPTION
MAJOR_REV(3:0)	Major revision number
MINOR_REV(3:0)	Minor revision number

11.2.2 VCORE_CTRL1 Register

Address: 0x02
Reset: 0x0C
Description: Control register for the VCORE dc-dc regulator. Maximum allowed value for VCORE_VOLT(4:0) is 0x12. Any attempt to write a value higher than the maximum results in 0x12 being written instead. See Appendix A for more details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	HW_nSW	STEP_nJMP	BYP_COMP	VCORE_VOLT(4:0)				
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	1	1	0	0

FIELD NAME	DESCRIPTION
HW_nSW	0 = VCORE voltage controlled by software (VCORE_VOLT) 1 = VCORE voltage controlled by VMODE and PWROK pins
STEP_nJMP	This bit is only valid when HW_nSW = 1 0 = VCORE voltage changes between roof and floor in a single step 1 = VCORE voltage changes between roof and floor in multiple steps (programmable range)
BYP_COMP	This bit impacts the behavior of the PWROK signal only, and is only valid when HW_nSW=1. 0: Internal comparator is used during a transition 1: Internal comparator is disabled (always indicates that the voltage is within range)
VCORE_VOLT(4:0)	Controls the voltage (when HW_nSW = 0) of the VCORE regulator

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11.2.3 VCORE_CTRL2 Register

Address: 0x03
Reset: 0x05
Description: Control register for the VCORE dc-dc regulator. This register is only valid when HW_nSW = 1. See Appendix A for more details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	STEP_PER(7:0)							
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	1	0	1

FIELD NAME	DESCRIPTION
STEP_PER(7:0)	When STEP_nJMP = 0, used to set the additional time the PWROK signal is held low after VCORE changes from ROOF/FLOOR to FLOOR/ROOF When STEP_nJMP = 1, used to set the time between each step when VCORE voltage changes between ROOF and FLOOR

11.2.4 VCORE_CTRL3 Register

Address: 0x04
Reset: 0x02
Description: Control register for the VCORE dc-dc regulator. This register is only valid when HW_nSW = 1. Maximum allowed value for FLOOR(4:0) is 0x12. Any attempt to write a value higher than the maximum will result in 0x12 being written instead. See Appendix A for more details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	FLOOR(4:0)				
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	1	0

FIELD NAME	DESCRIPTION
FLOOR(4:0)	Sets the voltage floor of the VCORE regulator when being controlled by VMODE (HW_nSW = 1).

11.2.5 VCORE_CTRL4 Register

Address: 0x05
Reset: 0x0C
Description: Control register for the VCORE dc-dc regulator. This register is only valid when HW_nSW = 1. Maximum allowed value for ROOF(4:0) is 0x12. Any attempt to write a value higher than the maximum will result in 0x12 being written instead. See Appendix A for more details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	ROOF(4:0)				
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	1	1	0	0

FIELD NAME	DESCRIPTION
ROOF(4:0)	Sets the voltage roof of the VCORE regulator when being controlled by VMODE (HW_nSW = 1).

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11.2.6 VCORE_CTRL5 Register

Address: 0x06
Reset: 0x03
Description: Mode setting for the VCORE dc-dc regulator. See Table 3−1 for details. This register setting can be overridden by the hardware sleep control logic. See section 10.16 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	–	VCORE_MODE(1:0)	
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	1	1

FIELD NAME	DESCRIPTION
VCORE_MODE(1:0)	Sets the mode of the VCORE regulator. The VCORE_MODE bits are set automatically to 11 (0x03) when the TWL92230 device transitions to the M_Active state and are reset when the device transitions to either the M_WaitOn or M_Backup states (see section 10.5 for state definitions and diagrams). The VCORE_MODE bits are set also to 11 (0x03) at an nRESWARM event.

11.2.7 DCDC_CTRL1 Register

Address: 0x07
Reset: 0x33 (0x31) depending on boot mode.
Description: Voltage setting for the DCDC2 and DCDC3 regulators. See Table 3−4 and Table 3−5 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	DCDC3_VOLT(2:0)			DCDC2_VOLT(2:0)		
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	1	1	0	0 (0)	1 (0)	1 (1)

FIELD NAME	DESCRIPTION
DCDC3_VOLT(2:0)	Voltage setting for the DCDC3 regulator
DCDC2_VOLT(2:0)	Voltage setting for the DCDC2 regulator

11.2.8 DCDC_CTRL2 Register

Address: 0x08
Reset: 0x03
Description: Mode setting for the DCDC2 regulator. See Table 3−2 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	DCDC2_MODE(2:0)		
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	1	1

FIELD NAME	DESCRIPTION
DCDC2_MODE(2:0)	Sets the mode of the DCDC2 regulator. The DCDC2_MODE bits are set automatically to 011 when the TWL92230 device transitions to the M_Active state and are reset when the device transitions to either the M_WaitOn or M_Backup states (see section 10.5 for state definitions and diagrams). The DCDC2_MODE bits are set also to 011 at an nRESWARM event.

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11.2.9 DCDC_CTRL3 Register

Address: 0x09
Reset: 0x00
Description: Mode setting for the DCDC3 regulator. See Table 3−2 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	DCDC3_MODE(2:0)		
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
DCDC3_MODE(2:0)	Sets the mode of the DCDC3 regulator.

11.2.10 LDO_CTRL1 Register

Address: 0x0A
Reset: 0x95
Description: Voltage setting for the VMMC, VAUX, VIO, and VMEM regulators. See the VMMC, VAUX, VIO, and VMEM specifications for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	VMMC_VOLT(1:0)		VAUX_VOLT(1:0)		VIO_VOLT(1:0)		VMEM_VOLT(1:0)	
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	1	0	0	1	0	1	0	1

FIELD NAME	DESCRIPTION
VMMC_VOLT(1:0)	Controls the voltage of the VMMC regulator.
VAUX_VOLT(1:0)	Controls the voltage of the VAUX regulator.
VIO_VOLT(1:0)	Controls the voltage of the VIO regulator.
VMEM_VOLT(1:0)	Controls the voltage of the VMEM regulator.

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11.2.11 LDO_CTRL2 Register

Address: 0x0B
Reset: 0x7E
Description: Contains voltage setting for the VPLL regulator and the pulldown enable bits for VMMC, VAUX, VIO, VMEM, and VPLL regulators. See the VMMC, VAUX, VIO, VMEM, and VPLL specifications for details.

NOTE: These bits are reset whenever the TWL92230 device enters into the M_WaitOn or M_Backup states (see section 10.5 for state definitions and diagrams). Therefore, if a regulator normally does not use the pull−down, when the device enters into either the M_WaitOn or M_Backup state, the pull−down will be enabled at the transition into that state.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	−	VMMC_PDEN	VAUX_PDEN	VIO_PDEN	VMEM_PDEN	VPLL_PDEN	VPLL_VOLT(1:0)	
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	1	1	1	1	1	1	0

FIELD NAME	DESCRIPTION
VMMC_PDEN	0 = VMMC pulldown resistor disabled 1 = VMMC pulldown resistor enabled when VMMC_MODE = 00
VAUX_PDEN	0 = VAUX pulldown resistor disabled 1 = VAUX pulldown resistor enabled when VAUX_MODE = 00
VIO_PDEN	0 = VIO pulldown resistor disabled 1 = VIO pulldown resistor enabled when VIO_MODE = 00
VMEM_PDEN	0 = VMEM pulldown resistor disabled 1 = VMEM pulldown resistor enabled when VMEM_MODE = 00
VPLL_PDEN	0 = VPLL pulldown resistor disabled 1 = VPLL pulldown resistor enabled when VPLL_MODE = 00
VPLL_VOLT(1:0)	Controls the voltage of the VPLL regulator.

11.2.12 LDO_CTRL3 Register

Address: 0x0C
Reset: 0x00 (0x03) depending on boot mode, see description below
Description: Mode settings for the VMEM regulator. See Table 4−3 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	−	−	−	−	−	−	VMEM_MODE(1:0)	
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0 (1)	0 (1)

FIELD NAME	DESCRIPTION
VMEM_MODE(1:0)	Controls the mode of the VMEM regulator. When the TWL92230 device is booted in mode M_Config0, M_Config1, or M_Config2, the VMEM_MODE bits are set automatically to 11 (0x03) when the TWL92230 device transitions to the M_Active state and are reset when the device transitions to either the M_WaitOn or M_Backup states (see section 10.5 for state definitions and diagrams). The VMEM_MODE bits are set also to 11 (0x03) at an nRESWARM event if the device was booted in M_Config0, M_Config1 or M_Config2 modes. For M_Config3, the VMEM_MODE bits are set to 00 (0x00) for both cases.

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11.2.13 LDO_CTRL4 Register

Address: 0x0D
Reset: 0x00 (0x03) depending on boot mode, see description below
Description: Mode settings for the VIO regulator. See Table 4−2 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	–	VIO_MODE(1:0)	
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0 (1)	0 (1)

FIELD NAME	DESCRIPTION
VIO_MODE(1:0)	Controls the mode of the VIO regulator. When the TWL92230 device is booted in mode M_Config0, M_Config1, or M_Config2, the VIO_MODE bits are set automatically to 11 (0x03) when the TWL92230 device transitions to the M_Active state and are reset when the device transitions to either the M_WaitOn or M_Backup states (see section 10.5 for state definitions and diagrams). The VIO_MODE bits are set also to 11 (0x03) at an nRESWARM event if the device was booted in the M_Config0, M_Config1, or M_Config2 modes. For M_Config3, the VIO_MODE bits are set to 00 (0x00) for both cases.

11.2.14 LDO_CTRL5 Register

Address: 0x0E
Reset: 0x03
Description: Mode settings for the VPLL regulator. See Table 4−6 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	–	VPLL_MODE(1:0)	
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	1	1

FIELD NAME	DESCRIPTION
VPLL_MODE(1:0)	Controls the mode of the VPLL regulator. The VPLL_MODE bits are set automatically to 11 (0x03) when the TWL92230 device transitions to the M_Active state and are reset when the device transitions to either the M_WaitOn or M_Backup states (see section 10.5 for state definitions and diagrams). The VPLL_MODE bits are set also to 11 (0x03) at an nRESWARM event.

11.2.15 LDO_CTRL6 Register

Address: 0x0F
Reset: 0x00
Description: Mode settings for the VAUX regulator. See Table 4−5 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	–	VAUX_MODE(1:0)	
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
VAUX_MODE(1:0)	Controls the mode of the VAUX regulator.

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11.2.16 LDO_CTRL7 Register

Address: 0x10
Reset: 0x00
Description: Mode settings for the VMMC regulator. See Table 4−4 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	–	VMMC_MODE(1:0)	
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
VMMC_MODE(1:0)	Controls the mode of the VMMC regulator.

11.2.17 LDO_CTRL8 Register

Address: 0x11
Reset: 0x00
Description: Enable bits for the 0.5-V reference and the VADAC LDO.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	–	REF05_EN	VADAC_EN
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
REF05_EN	0 =0.5-V reference is off. 1 = 0.5-V reference is on.
VADAC_EN	0 = VADAC LDO is off. 1 = VADAC LDO is on.

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11.2.18 SLEEP_CTRL1 Register

Address: 0x12
Reset: 0x00
Description: Allows VMODE to control the mode of the regulators, overriding the xxx_MODE(x:0) settings for the ON mode of the corresponding regulators. If the regulator was not in the ON mode, it remains in the mode it was in even when the corresponding SLPEN1 bit is set. This control is independent of the sleep control function of GPIO3 and is ORed with that function. See section 10.15 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	VPLL_ SLPEN1	VMMC_ SLPEN1	VAUX_ SLPEN1	VIO_ SLPEN1	VMEM_ SLPEN1	DC3_ SLPEN1	DC2_ SLPEN1	VC_ SLPEN1
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
VPLL_SLPEN1	0 = VPLL state controlled by VPLL_MODE(1:0) 1 = VPLL state is forced to sleep if VPLL_MODE = on and VMODE = 0
VMMC_SLPEN1	0 = VMMC state controlled by VMMC_MODE(1:0) 1 = VMMC state is forced to sleep if VMMC_MODE = active and VMODE = 0
VAUX_SLPEN1	0 = VAUX state controlled by VAUX_MODE(1:0) 1 = VAUX state is forced to sleep if VAUX_MODE = active and VMODE = 0
VIO_SLPEN1	0 = VIO state controlled by VIO_MODE(1:0) 1 = VIO state is forced to sleep if VIO_MODE = active and VMODE = 0
VMEM_SLPEN1	0 = VMEM state controlled by VMEM_MODE(1:0) 1 = VMEM state is forced to sleep if VMEM_MODE = active and VMODE = 0
DC3_SLPEN1	0 = DC3 state controlled by DCDC3_MODE(1:0) 1 = DC3 state is forced to sleep if DC3_MODE = active and VMODE = 0
DC2_SLPEN1	0 = DC2 state controlled by DCDC2_MODE(1:0) 1 = DC2 state is forced to sleep if DC2_MODE = active and VMODE = 0
VC_SLPEN1	0 = VC state controlled by VCORE_MODE(1:0) 1 = VC state is forced to sleep if VC_MODE = active and VMODE = 0

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11.2.19 SLEEP_CTRL2 Register

Address: 0x13
Reset: 0x00
Description: Allows GPIO3 to control the mode of the regulators, overriding the xxx_MODE(x:0) settings for the ON mode of the corresponding regulators. If the regulator was not in the ON mode, it remains in the mode it was in even when the corresponding SLPEN2 bit is set. This control is independent of the sleep control function of VMODE and is ORed with that function. The alternate function for GPIO3 must be selected with the SLPCTLEN bit in the GPIO_CTRL register. See section 10.15 for details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	VPLL_ SLPEN2	VMMC_ SLPEN2	VAUX_ SLPEN2	VIO_ SLPEN2	VMEM_ SLPEN2	DC3_ SLPEN2	DC2_ SLPEN2	VC_ SLPEN2
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
VPLL_SLPEN2	0 = VPLL state controlled by VPLL_MODE(1:0) 1 = VPLL state is forced to sleep if VPLL_MODE = on and GPIO3 = 0[1]
VMMC_SLPEN2	0 = VMMC state controlled by VMMC_MODE(1:0) 1 = VMMC state is forced to sleep if VMMC_MODE = active and GPIO3 = 0[1]
VAUX_SLPEN2	0 = VAUX state controlled by VAUX_MODE(1:0) 1 = VAUX state is forced to sleep if VAUX_MODE = active and GPIO3 = 0[1]
VIO_SLPEN2	0 = VIO state controlled by VIO_MODE(1:0) 1 = VIO state is forced to sleep if VIO_MODE = active and GPIO3 = 0[1]
VMEM_SLPEN2	0 = VMEM state controlled by VMEM_MODE(1:0) 1 = VMEM state is forced to sleep if VMEM_MODE = active and GPIO3 = 0[1]
DC3_SLPEN2	0 = DC3 state controlled by DCDC3_MODE(1:0) 1 = DC3 state is forced to sleep if DC3_MODE = active and GPIO3 = 0[1]
DC2_SLPEN2	0 = DC2 state controlled by DCDC2_MODE(1:0) 1 = DC2 state is forced to sleep if DC2_MODE = active and GPIO3 = 0[1]
VC_SLPEN2	0 = VC state controlled by VCORE_MODE(1:0) 1 = VC state is forced to sleep if VC_MODE = active and GPIO3 = 0[1]

1. The alternate function for GPIO3 must be selected with the SLPCTLEN bit in the GPIO_CTRL register.

11.2.20 DEVICE_OFF Register

Address: 0x14
Reset: 0x00
Description: Software shutdown for TWL92230. This is a self-clearing bit. This register is only valid for M_Config1.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	–	–	DEVOFF
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
DEVOFF	0 = Normal operation 1 = TWL92230 shutdown sequence initiated

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11.2.21 OSC_CTRL Register

Address: 0x15
Reset: 0x01
Description: Control for the 32-kHz crystal oscillator and the internal high-frequency oscillator.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK32K_GOOD	–	–	–	–	HFCLK_SEL[1:0]		CLK32K_OUT
Read/Write	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	x	0	0	0	0	0	0	1

FIELD NAME	DESCRIPTION
CLK32K_GOOD	This bit is valid only when the 32KDETEN pin is set high (32-kHz duty-cycle detection enabled) 0: The 32-kHz clock coming from the internal crystal oscillator (crystal mode or feed-through mode) has not met the minimum duty-cycle criteria 1: The 32-kHz clock coming from the internal crystal oscillator (crystal mode or feed-through mode) has met the minimum duty-cycle criteria
HFCLK_SEL[1:0]	Sets the frequency of the signal to be applied to the HFCLK pin 00: No clock 01: 12 MHz 10: 13 MHz 11: 19.2 MHz
CLK32K_OUT	0 = 32KOUT pin is held low 1 = Internal 32-kHz clock is driven onto the 32KOUT pin.

11.2.22 DETECT_CTRL Register

Address: 0x16
Reset: 0x09
Description: Debounce time settings for the detector circuits.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	UVLO_BYP/ UVLO_EN	UVLODB_PER(2:0)			LBDB_PER(2:0)		
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	1	0	0	1

FIELD NAME	DESCRIPTION
Versions prior to PG2.2 UVLO_BYP	UVLO falling threshold bypass – This applies for M_Config3 only (see section 10.4). 0: UVLO falling event shuts down all TWL92230 regulators. 1: UVLO falling event is bypassed (ignored). All regulators remain in the mode they were in prior to the UVLO falling event.
PG2.2 and later versions UVLO_EN	UVLO falling threshold enable – This applies for M_Config3 only (see section 10.4). 0: UVLO falling event is bypassed (ignored). All regulators remain in the mode they were in prior to the UVLO falling event. This is the default state at startup. 1: UVLO falling event shuts down all TWL92230 regulators.
UVLODB_PER(2:0)	UVLO detector debounce period T_{DB} = LBDB_PER × 100 µs
LBDB_PER(2:0)	Low Battery detector debounce period T_{DB} = LBDB_PER × 100 µs

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11.2.23 INT_MASK1 Register

Address: 0x17
Reset: 0xFF
Description: Contains the interrupt mask bits for maskable interrupts. Masking the interrupt will inhibit the INT signal going low due to that interrupt but will not inhibit the status bit from being set due to an event/condition.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	TSHUT_ MSK	UVLO_ MSK	HOTDIE_ MSK	LOWBAT_ MSK	S2D1_MSK	S1D1_MSK	S2CD_MSK	S1CD_MSK
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	1	1	1	1	1	1	1	1

FIELD NAME	DESCRIPTION
TSHUT_MSK	0 = Thermal shutdown detection interrupt unmasked 1 = Thermal shutdown detection interrupt masked
UVLO_MSK	0 = UVLO detection interrupt unmasked 1 = UVLO detection interrupt masked
HOTDIE_MSK	0 = Hot die detection interrupt unmasked 1 = Hot die detection interrupt masked
LOWBAT_MSK	0 = Low battery detection interrupt unmasked 1 = Low battery detection interrupt masked
S2D1_MSK	0 = DATA1 low detection on SLOT2 interrupt unmasked 1 = DATA1 low detection on SLOT2 interrupt masked
S2D1_MSK	0 = DATA1 low detection on SLOT1 interrupt unmasked 1 = DATA1 low detection on SLOT1 interrupt masked
S2CD_MSK	0 = Slot 2 detection interrupt unmasked 1 = Slot 2 detection interrupt masked
S1CD_MSK	0 = Slot 1 detection interrupt unmasked 1 = Slot 1 detection interrupt masked

11.2.24 INT_MASK2 Register

Address: 0x18
Reset: 0x0F
Description: Contains the interrupt mask bits for maskable interrupts. Masking the interrupt will inhibit the INT signal going low due to that interrupt but will not inhibit the status bit from being set due to an event/condition.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	PSHBTN_MSK	RTCERR_MSK	RTCALM_MSK	RTCTMR_MSK
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	1	1	1	1

FIELD NAME	DESCRIPTION
PSHBTN_MSK	0 = Pushbutton interrupt unmasked 1 = Pushbutton interrupt masked (this will not inhibit a power up sequence)
RTCERR_MSK	0 = RTC error interrupt unmasked 1 = RTC error interrupt masked
RTCALM_MSK	0 = RTC alarm interrupt unmasked 1 = RTC alarm interrupt masked
RTCTMR_MSK	0 = RTC timer interrupt unmasked 1 = RTC timer interrupt masked

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11.2.25 INT_STATUS1 Register

Address: 0x19
Reset: N/A
Description: Contains the interrupt status flags for maskable interrupts. See section 8.13 for more info.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	TSHUT	UVLO	HOTDIE	LOWBAT	S2D1	S1D1	S2CD	S1CD
Read/Write	r	r	r	r	r	r	r	r

FIELD NAME	DESCRIPTION
TSHUT	0 = No interrupt has occurred 1 = A thermal shutdown event has occurred(1)
UVLO	0 = No interrupt has occurred 1 = An undervoltage lockout condition has occurred(1)
HOTDIE	0 = No interrupt has occurred 1 = A hot die condition has occurred
LOWBAT	0 = No interrupt has occurred 1 = A low battery condition has occurred
S2D1	0 = No interrupt has occurred 1 = An SDIO condition has occurred on memcard Slot2
S1D1	0 = No interrupt has occurred 1 = An SDIO condition has occurred on memcard Slot1
S2CD	0 = No interrupt has occurred 1 = A memcard insertion or removal has been detected on Slot 2
S1CD	0 = No interrupt has occurred 1 = A memcard insertion or removal has been detected on Slot 1

(1) A UVLO or TSHUT interrupt causes the immediate shutdown of all noncritical circuits including the VCORE regulator (UVLO shutdown may be inhibited). The external signal nRESPWRON is asserted, and all TWL92230 registers except RTC and interrupt status registers are reset to their default condition. However, the status of the UVLO or TSHUT event is remembered as the internal regulator VDIG continues to operate.

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11.2.26 INT_STATUS2 Register

Address: 0x1A
Reset: N/A
Description: Contains the interrupt status flags for maskable interrupts.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	PSHBTN	RTCERR	RTCALM	RTCTMR
Read/Write	r	r	r	r	r	r	r	r

FIELD NAME	DESCRIPTION
PSHBTN	0 = No interrupt has occurred 1 = A Pushbutton event has occurred.*
RCERR	0 = No interrupt has occurred 1 = An RTC error event has occurred
RTCALM	0 = No interrupt has occurred 1 = An RTC alarm event has occurred
RTCTMR	0 = No interrupt has occurred 1 = An RTC timer event has occurred

1. Pushbutton events are only valid in the M_Config1 boot mode. Only a pushbutton event that occurs while the device is powered up (M_Active or M_LowVolt) will cause an interrupt. A pushbutton event that occurs while the device is off (M_WaitOn) will cause the device to turn on. No interrupt will be generated for such an event.

11.2.27 INT_ACK1 Register

Address: 0x1B
Reset: 0x00
Description: These bits are self-clearing and always read 0s. When written with a 1, the corresponding interrupt status flag is cleared. Writing a 0 has no effect.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	TSHUT_ ACK	UVLO _ACK	HOTDIE _ACK	LOWBAT _ACK	S2D1_ACK	S1D1_ACK	S2CD _ACK	S1CD _ACK
Read/Write	w	w	w	w	w	w	w	w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
TSHUT_ACK	Acknowledge bit for the thermal shutdown status flag
UVLO_ACK	Acknowledge bit for the under-voltage lockout status flag
HOTDIE_ACK	Acknowledge bit for the hot die status flag
LOWBAT_ACK	Acknowledge bit for the low battery status flag
S2D1_ACK	Acknowledge bit for the SDIO2 status flag
S1D1_ACK	Acknowledge bit for the SDIO1 status flag
S2CD_ACK	Acknowledge bit for the Slot 2 insertion event status flag
S1CD_ACK	Acknowledge bit for the Slot 1 insertion event status flag

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11.2.28 INT_ACK2 Register

Address: 0x1C
Reset: 0x00
Description: These bits are self-clearing and always read 0s. When written with a 1, the corresponding interrupt status flag is cleared. Writing a 0 has no effect.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	PSHBTN_ACK	RTCERR_ACK	RTCALM_ACK	RTCTMR_ACK
Read/Write	w	w	w	w	w	w	w	w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
PSHBTN_ACK	Acknowledge bit for the Pushbutton event status flag
RTCERR_ACK	Acknowledge bit for the RTC error event status flag
RTCALM_ACK	Acknowledge bit for the RTC alarm event status flag
RTCTMR_ACK	Acknowledge bit for the RTC timer event status flag

11.2.29 GPIO_CTRL Register

Address: 0x1D
Reset: 0x07
Description: Control register for the GPIO ports.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	SLPCTLEN	SLOTSELEN	–	–	GPIO_DIR(3:1)		
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	1	1	1

FIELD NAME	DESCRIPTION
SLPCTLEN	0 = Sleep control functionality on GPIO3 is disabled 1 = Sleep control functionality on GPIO3 is enabled and GPIO3 direction overridden to an input
SLOTSELEN	0 = This alternate function for GPIO2 is disabled. 1 = This alternate function for GPIO2 is enabled: GPIO2 becomes an input (SLOT_SEL) that selects the MCT slot. SLOT_SEL=0: Slot 1 is selected and SLOT_SEL=1: Slot 2 is selected
GPIO_DIR(3:1)	Sets the direction of each individual GPIO pin of TWL92230. 0 = GPIO pin is an output 1 = GPIO pin is an input

11.2.30 GPIO_IN Register

Address: 0x1E
Reset: NA
Description: Input register for GPIO pins.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	GPIO_IN(3:1)		
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	x	x	x

FIELD NAME	DESCRIPTION
GPIO_IN(3:1)	Indicates the state of the GPIO pin, regardless of the direction of the pin.

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11.2.31 GPIO_OUT Register

Address: 0x1F
Reset: 0x00
Description: Output register for GPIO pins.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	GPIO_OUT(3:1)		
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
GPIO_OUT(3:1)	Set the state of the GPIO pin when that pin is configured as an output.

11.2.32 BBSMS Register

Address: 0x20
Reset: 0x00
Description: Control register for the backup battery switch and monitoring system.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	BBSEL(1:0)		BBSW	BBCHEN
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
BBSEL(1:0)	Selection for target backup battery fully charged voltage
BBSW	Backup battery switch position (read only). This bit will normally always be read as a 0 since a 1 would indicate we are in the M_Backup state, in which no I2C reads can occur. 0 = LDO6 supply is the main battery 1 = LDO6 supply is the backup battery
BBCHEN	0 = Backup battery charge is disabled 1 = Backup battery charge is enabled

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11.2.33 RTC_CTRL Register

Address: 0x21
Reset: 0x00
Description: Register containing RTC configuration bits.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	EVERY(1:0)		MODE12_n24	RTC_AL_EN	RTC_EN
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
EVERY(1:0)	Selection for RTC timer event interval: 00 = Event occurs every second 01 = Event occurs every minute 10 = Event occurs every hour 11 = Event occurs every day
MODE12_n24	Selects hour format 0 = 24-hour mode 1 = 12-hour mode (AM/PM mode)
RTC_AL_EN	0 = RTC alarm is disabled 1 = RTC alarm is enabled
RTC_EN	0 = RTC is disabled 1 = RTC is enabled

11.2.34 RTC_UPDATE Register

Address: 0x22
Reset: 0x00
Description: This register contains the timer and calendar update command. The RTC_SEC, RTC_MIN … RTC_YR registers are written with the data to be updated before writing the RTC_UPDATE register. Once the update has occurred, this register is cleared.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	UPDATE_TC(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
UPDATE_TC(3:0)	0000 = No update 0001 = Update seconds 0010 = Update minutes 0011 = Update hours 0100 = Update days 0101 = Update months 0110 = Update years 0111 = Update week day 1000 = Update everythIng 1xxx = Reserved (Do not use)

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11.2.35 RTC_SEC Register

Address: 0x23
Reset: 0x00
Description: BCD seconds information. Reading this register returns the RTC counter data. Writing this register loads the update registers, but has no effect until the RTC_UPDATE register is written.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	SEC1(2:0)			SEC0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
SEC1(2:0)	First digit of seconds. Valid values are 0 to 5.
SEC0(3:0)	Second digit of seconds. Valid values are 0 to 9.

11.2.36 RTC_MIN Register

Address: 0x24
Reset: 0x00
Description: BCD minutes information. Reading this register returns the RTC counter data. Writing this register loads the update registers, but has no effect until the RTC_UPDATE register is written.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	MIN1(2:0)			MIN0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
MIN1(2:0)	First digit of minutes. Valid values are 0 to 5.
MIN0(3:0)	Second digit of minutes. Valid values are 0 to 9.

11.2.37 RTC_HR Register

Address: 0x25
Reset: 0x00
Description: BCD hours and AM/PM information. Reading this register returns the RTC counter data. Writing this register loads the update registers, but has no effect until the RTC_UPDATE register is written.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	PM_nAM	–	HOUR1(1:0)		HOUR0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
PM_nAM	0 = AM 1 = PM
HOUR1(1:0)	First digit of hours. Valid values are 0 to 2.
HOUR0(3:0)	Second digit of hours. Valid values are 0 to 9.

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11.2.38 RTC_DAY Register

Address: 0x26
Reset: 0x01
Description: BCD days information. Reading this register returns the RTC counter data. Writing this register loads the update registers, but has no effect until the RTC_UPDATE register is written.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	DAY1(1:0)		DAY0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	1

FIELD NAME	DESCRIPTION
DAY1(1:0)	First digit of days. Valid values are 0 to 3.
DAY0(3:0)	Second digit of days. Valid values are 0 to 9.

11.2.39 RTC_MON Register

Address: 0x27
Reset: 0x01
Description: BCD months information (01 –> January, 02 –> February, … 12 –> December). Reading this register returns the RTC counter data. Writing this register loads the update registers, but has no effect until the RTC_UPDATE register is written.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	MONTH1	MONTH0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	1

FIELD NAME	DESCRIPTION
MONTH1(1:0)	First digit of months. Valid values are 0 to 1.
MONTH0(3:0)	Second digit of months. Valid values are 0 to 9.

11.2.40 RTC_YR Register

Address: 0x28
Reset: 0x04
Description: BCD years information. Reading this register returns the RTC counter data. Writing this register loads the update registers, but has no effect until the RTC_UPDATE register is written.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	YEAR1(3:0)				YEAR0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	1	0	0

FIELD NAME	DESCRIPTION
YEAR1(3:0)	First digit of years. Valid values are 0 to 9.
YEAR0(3:0)	Second digit of years. Valid values are 0 to 9.

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11.2.41 RTC_WKDAY Register

Address: 0x29
Reset: 0x04
Description: Weekday information. Reading this register returns the RTC counter data. Writing this register loads the update registers, but has no effect until the RTC_UPDATE register is written.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	–	WEEKDAY(2:0)		
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	1	0	0

FIELD NAME	DESCRIPTION
WEEKDAY(2:0)	Day of week. Valid values are 0 to 6.

11.2.42 RTC_AL_SEC Register

Address: 0x2A
Reset: 0x00
Description: BCD seconds information. Sets the data to be compared against the counters for RTC alarm function. The RTC_AL_EN bit must be set for alarm functionality.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	AL_SEC1(2:0)			AL_SEC0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
AL_SEC1(2:0)	First digit of seconds. Valid values are 0 to 5.
AL_SEC0(3:0)	Second digit of seconds. Valid values are 0 to 9.

11.2.43 RTC_AL_MIN Register

Address: 0x2B
Reset: 0x00
Description: BCD minutes information. Sets the data to be compared against the counters for RTC alarm function. The RTC_AL_EN bit must be set for alarm functionality.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	AL_MIN1(2:0)			AL_MIN0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
AL_MIN1(2:0)	First digit of minutes. Valid values are 0 to 5.
AL_MIN0(3:0)	Second digit of minutes. Valid values are 0 to 9.

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11.2.44 RTC_AL_HR Register

Address: 0x2C
Reset: 0x00
Description: BCD hours and AM/PM information. Sets the data to be compared against the counters for RTC alarm function. The RTC_AL_EN bit must be set for alarm functionality.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	AL_PM_nAM	–	AL_HOUR1(1:0)		AL_HOUR0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
AL_PM_nAM	0 = AM 1 = PM
AL_HOUR1(1:0)	First digit of hours. Valid values are 0 to 2.
AL_HOUR0(3:0)	Second digit of hours. Valid values are 0 to 9.

11.2.45 RTC_AL_DAY Register

Address: 0x2D
Reset: 0x01
Description: BCD days information. Sets the data to be compared against the counters for the RTC alarm function. The RTC_AL_EN bit must be set for alarm functionality.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	AL_DAY1(1:0)		AL_DAY0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	1

FIELD NAME	DESCRIPTION
AL_DAY1(1:0)	First digit of days. Valid values are 0 to 3.
AL_DAY0(3:0)	Second digit of days. Valid values are 0 to 9.

11.2.46 RTC_AL_MON Register

Address: 0x2E
Reset: 0x01
Description: BCD months information (01 −> January, 02 −> February, … 12 −> December). Sets the data to be compared against the counters for RTC alarm function. The RTC_AL_EN bit must be set for alarm functionality.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	AL_MONTH1	AL_MONTH0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	1

FIELD NAME	DESCRIPTION
AL_MONTH1(1:0)	First digit of months. Valid values are 0 to 1.
AL_MONTH0(3:0)	Second digit of months. Valid values are 0 to 9.

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11.2.47 RTC_AL_YR Register

Address: 0x2F
Reset: 0x04
Description: BCD years information. Sets the data to be compared against the counters for RTC alarm function. The RTC_AL_EN bit must be set for alarm functionality.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	AL_YEAR1(3:0)				AL_YEAR0(3:0)			
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	1	0	0

FIELD NAME	DESCRIPTION
AL_YEAR1(3:0)	First digit of years. Valid values are 0 to 9.
AL_YEAR0(3:0)	Second digit of years. Valid values are 0 to 9.

11.2.48 RTC_COMP_MSB Register

Address: 0x30
Reset: 0x00
Description: MSB of RTC auto compensation value. The 16-bit 2s complement value comprised of RTC_COMP_MSB and RTC_COMP_LSB will be added to (or subtracted from if negative) the 32-kHz counter every hour.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTC_COMPH(7:0)							
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
RTC_COMPH(7:0)	MSB of the compensation value. 0x8000 and 0x8001 are not valid.

11.2.49 RTC_COMP_LSB Register

Address: 0x31
Reset: 0x00
Description: LSB of RTC auto compensation value. The 16-bit 2s complement value comprised of RTC_COMP_MSB and RTC_COMP_LSB will be added to (or subtracted from if negative) the 32-kHz counter every hour.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTC_COMPL(7:0)							
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
RTC_COMPL(7:0)	LSB of the compensation value. 0x8000 and 0x8001 are not valid.

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11.2.50 S1_PULL_EN Register

Address: 0x32
Reset: 0x00
Description: SLOT1 interface port pullup/pulldown enable register. Direction (up or down) determined by the S1_PULL_DIR register bits.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	S1_APPCLKF_DLY(2:0)			S1_CMD_EN	S1_DAT3_EN	S1_DAT2_EN	S1_DAT1_EN	S1_DAT0_EN
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
S1_APPCLKF_DLY(2:0)	Sets the programmable delay on the SLOT1 clock feedback path when SLOT1 or broadcast mode is selected. See chapter 8.23.2 for detail delay information.
S1_CMD_EN	1 = Enable pullup/pulldown on MC.S1CMD pin 0 = No pullup/pulldown selected
S1_DAT3_EN	1 = Enable pullup/pulldown on MC.S1DAT3 pin 0 = No pullup/pulldown selected
S1_DAT2_EN	1 = Enable pullup/pulldown on MC.S1DAT2 pin 0 = No pullup/pulldown selected
S1_DAT1_EN	1 = Enable pullup/pulldown on MC.S1DAT1 pin 0 = No pullup/pulldown selected
S1_DAT0_EN	1 = Enable pullup/pulldown on MC.S1DAT0 pin 0 = No pullup/pulldown selected

11.2.51 S1_PULL_DIR Register

Address: 0x33
Reset: 0x00
Description: SLOT1 interface port pullup/pulldown selection register. Pullup/pulldown resistor enable state determined by the S1_PULL_EN register bits.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	S1_CMD_UP	S1_DAT3_UP	S1_DAT2_UP	S1_DAT1_UP	S1_DAT0_UP
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
S1_CMD_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected
S1_DATA3_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected
S1_DATA2_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected
S1_DATA1_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected
S1_DATA0_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected

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11.2.52 S2_PULL_EN Register

Address: 0x34
Reset: 0x00
Description: SLOT2 interface port pullup/pulldown enable register. Direction (up or down) determined by the S2_PULL_DIR register bits.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	S2_APPCLKF_DLY(2:0)			S2_CMD_EN	S2_DAT3_EN	S2_DAT2_EN	S2_DAT1_EN	S2_DAT0_EN
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
S2_APPCLKF_DLY(2:0)	Sets the programmable delay on the SLOT2 clock feedback path when SLOT2 mode is selected. See chapter 8.23.2 for detail delay information.
S2_CMD_EN	1 = Enable pullup/pulldown on MC.S2CMD pin 0 = No pullup/pulldown selected
S2_DAT3_EN	1 = Enable pullup/pulldown on MC.S2DAT3 pin 0 = No pullup/pulldown selected
S2_DAT2_EN	1 = Enable pullup/pulldown on MC.S2DAT2 pin 0 = No pullup/pulldown selected
S2_DAT1_EN	1 = Enable pullup/pulldown on MC.S2DAT1 pin 0 = No pullup/pulldown selected
S2_DAT0_EN	1 = Enable pullup/pulldown on MC.S2DAT0 pin 0 = No pullup/pulldown selected

11.2.53 S2_PULL_DIR Register

Address: 0x35
Reset: 0x00
Description: SLOT2 interface port pullup/pulldown selection register. Pullup/pulldown resistor enable state determined by the S2_PULL_EN register bits.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	S2_CMD_UP	S2_DAT3_UP	S2_DAT2_UP	S2_DAT1_UP	S2_DAT0_UP
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
S2_CMD_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected
S2_DATA3_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected
S2_DATA2_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected
S2_DATA1_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected
S2_DATA0_UP	0 = Pulldown resistor selected 1 = Pullup resistor selected

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11.2.54 MCT_CTRL1 Register

Address: 0x36
Reset: 0x03
Description: Configuration register for MCT (Memory Card Transceiver) block. See MCT section for more details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	APBUFDRV	S2BUFDRV	S1BUFDRV	S2_CMD_OD	S1_CMD_OD	S2CD_SWNO	S1CD_SWNO
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	1	1

FIELD NAME	DESCRIPTION
APBUFDRV	0 = Application processor output buffer strength – 6 ns/10 pF 1 = Application processor output buffer strength – 3 ns/10 pF
S2BUFDRV	0 = SLOT2 output buffer strength – 6 ns/30 pF 1 = SLOT2 output buffer strength – 3 ns/30 pF
S1BUFDRV	0 = SLOT1 output buffer strength – 6 ns/30 pF 1 = SLOT1 output buffer strength – 3 ns/30 pF
S2_CMD_OD	0 = SLOT2 CMD buffer is push−pull type 1 = SLOT2 CMD buffer is open−drain type
S1_CMD_OD	0 = SLOT1 CMD buffer is push−pull type 1 = SLOT1 CMD buffer is open−drain type
S2CD_SWNO	0 = SLOT2 card detect switch is normally closed. 1 = SLOT2 card detect switch is normally open.
S1CD_SWNO	0 = SLOT1 card detect switch is normally closed. 1 = SLOT1 card detect switch is normally open.

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11.2.55 MCT_CTRL2 Register

Address: 0x37
Reset: 0xC0
Description: Configuration register for MCT (memory card transceiver) block. See MCT section for more details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	S2CD_ DBEN	S1CD_ DBEN	S2CD_ BUFEN	S1CD_ BUFEN	S2D1_ BUFEN	S1D1_ BUFEN	VS2_SEL[1:0]	
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	1	1	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
S2CD_DBEN	0 = SLOT2 CD (Card Detect) signal debounce disabled 1 = SLOT2 CD (Card Detect) signal debounce enabled
S1CD_DBEN	0 = SLOT1 CD (Card Detect) signal debounce disabled 1 = SLOT1 CD (Card Detect) signal debounce enabled
S2CD_BUFEN	0 = SLOT2 CD (Card Detect) interrupt detection disabled 1 = SLOT2 CD (Card Detect) interrupt detection enabled (Buffer permanently enabled)
S1CD_BUFEN	0 = SLOT1 CD (Card Detect) interrupt detection disabled 1 = SLOT1 CD (Card Detect) interrupt detection enabled (Buffer permanently enabled)
S2D1_BUFEN	0 = SLOT2 DATA1 input buffer disabled 1 = SLOT2 DATA1 input buffer enabled
S1D1_BUFEN	0 = SLOT1 DATA1 input buffer disabled 1 = SLOT1 DATA1 input buffer enabled
VS2_SEL[1:0]	00: SLOT2 is powered by DCDC3 01: SLOT2 is powered by VAUX 1x: SLOT2 is powered by an external source

11.2.56 MCT_CTRL3 Register

Address: 0x38
Reset: 0x00
Description: Configuration register for MCT (memory card transceiver) block. See MCT section for more details.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	S2_AUTO_ EN	S1_AUTO_ EN	SLOT2_ EN	SLOT1_ EN
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

FIELD NAME	DESCRIPTION
S2_AUTO_EN	0 = SLOT2 Autonomous shutdown is disabled. 1 = SLOT2 Autonomous shutdown is enabled.
S1_AUTO_EN	0 = SLOT1 Autonomous shutdown is disabled. 1 = SLOT1 Autonomous shutdown is enabled.
SLOT2_ EN	0: SLOT2 is disabled. 1: SLOT2 is enabled.
SLOT1_ EN	0: SLOT1 is disabled. 1: SLOT1 is enabled.

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11.2.57 MCT_PIN_ST Register

Address: 0x39
Reset: NA
Description: This register contains bits that reflect the state of the specific MCT pins. If these pins have a debounce option and that option is enabled, the corresponding bit will reflect the debounced signal.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	–	–	S2_DAT1_ ST	S1_DAT1_ ST	S2_CD_ ST	S1_CD_ ST
Read/Write	r	r	r	r	r	r	r	r
Reset Value	–	–	–	–	–	–	–	–

FIELD NAME	DESCRIPTION
S2_DAT1_ST	Reflects the state of the SLOT2 DATA1 pin.
S1_DAT1_ST	Reflects the state of the SLOT1 DATA1 pin.
S2_CD_ST	Reflects the state of the SLOT2 CD pin.
S1_CD_ST	Reflects the state of the SLOT1 CD pin.

11.2.58 DEBOUNCE1 Register

Address: 0x3A
Reset: 0x05
Description Debounce interval setting for nRESWARM signal

	D7	D6	D5	D4	D3	D2	D1	D0
Name	–	–	RESWARM_DB[5:0]					
Read/Write	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	1	0	1

FIELD NAME	DESCRIPTION
RESWARM_DB[5:0]	Sets the debounce interval for the nRESWARM signal. T = RESWARM_DB*10 µs

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11.3 Register Map

Table 11−2. TWL92230 Register Map

ADDRESS (HEX)	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	ACCESS TYPE	RESET (HEX)
0x01	REVISION	MAJOR_REV(3:0)				MINOR_REV(3:0)				R	0xXY
0x02	VCORE_CTRL1	HW_nSW	STEP_nJMP	BYP_COMP	VCORE_VOLT(4:0)					RW	0x0C
0x03	VCORE_CTRL2	STEP_PER(7:0)								RW	0x05
0x04	VCORE_CTRL3	–	–	–	FLOOR(4:0)					RW	0x02
0x05	VCORE_CTRL4	–	–	–	ROOF(4:0)					RW	0x0C
0x06	VCORE_CTRL5	–	–	–	–	–	–	VCORE_MODE(1:0)		RW	0x03
0x07	DCDC_CTRL1	–	–	DCDC3_VOLT(2:0)			DCDC2_VOLT(2:0)			RW	$0x33_1$
0x08	DCDC_CTRL2	–	–	–	–	–	DCDC2_MODE(2:0)			RW	0x03
0x09	DCDC_CTRL3	–	–	–	–	–	DCDC3_MODE(2:0)			RW	0x00
0x0A	LDO_CTRL1	VMMC_VOLT(1:0)		VAUX_VOLT(1:0)		VIO_VOLT(1:0)		VMEM_VOLT(1:0)		RW	0x95
0x0B	LDO_CTRL2	–	VMMC_PDEN	VAUX_PDEN	VIO_PDEN	VMEM_PDEN	VPLL_PDEN	VPLL_VOLT(1:0)		RW	0x7E
0x0C	LDO_CTRL3	–	–	–	–	–	–	VMEM_MODE(1:0)		RW	0x03(2)
0x0D	LDO_CTRL4	–	–	–	–	–	–	VIO_MODE(1:0)		RW	0x03(3)
0x0E	LDO_CTRL5	–	–	–	–	–	–	VPLL_MODE(1:0)		RW	0x00
0x0F	LDO_CTRL6	–	–	–	–	–	–	VAUX_MODE(1:0)		RW	0x00
0x10	LDO_CTRL7	–	–	–	–	–	–	VMMC_MODE(1:0)		RW	0x00
0x11	LDO_CTRL8	–	–	–	–	–	–	REF05_EN	VADAC_EN	RW	0x00
0x12	SLEEP_CTRL1	VPLLSLPEN1	VMMCSLPEN1	VAUXSLPEN1	VIOSLPEN1	VMEMSLPEN1	DC3SLPEN1	DC2SLPEN1	VCSLPEN1	RW	0x00
0x13	SLEEP_CTRL2	VPLLSLPEN2	VMMCSLPEN2	VAUXSLPEN2	VIOSLPEN2	VMEMSLPEN2	DC3SLPEN2	DC2SLPEN2	VCSLPEN2	RW	0x00
0x14	DEVICE_OFF	–	–	–	–	–	–	–	DEVOFF	W	0x00
0x15	OSC_CTRL	CLK32K_GOOD	–	–	–	–	HFCLK_SEL(1:0)		CLK32K_OUT	RW	0x01
0x16	DETECT_CTRL	–	UVLO_BYP/ UVLO_EN(4)	UVLODB_PER(2:0)			LBDB_PER(2:0)			RW	0x09
0x17	INT_MASK1	TSHUT_MSK	UVLO_MSK	HOTDIE_MSK	LOWBAT_MSK	S2D1_MSK	S1D1_MSK	S2CD_MSK	S1CD_MSK	RW	0xFF
0x18	INT_MASK2	–	–	–	–	PSHBTN_MSK	RTCERR_MSK	RTCALM_MSK	RTCTMR_MSK	RW	0x0F
0x19	INT_STATUS1	TSHUT	UVLO	HOTDIE	LOWBAT	S2D1	S1D1	S2CD	S1CD	R	0x00
0x1A	INT_STATUS2	–	–	–	–	PSHBTN	RTCERR	RTCALM	RTCTMR	R	0x00
0x1B	INT_ACK1	TSHUT_ACK	UVLO_ACK	HOTDIE_ACK	LOWBAT_ACK	S2D1_ACK	S1D1_ACK	S2CD_ACK	S1CD_ACK	W	0x00
0x1C	INT_ACK2	–	–	–	–	PSHBTN_ACK	RTCERR_ACK	RTCALM_ACK	RTCTMR_ACK	W	0x00
0x1D	GPIO_CTRL	–	SLPCTLEN	SLOTSELEN	–	–	GPIO_DIR(3:1)			RW	0x07
0x1E	GPIO_IN	–	–	–	–	–	GPIO_IN(3:1)			R	0x00
0x1F	GPIO_OUT	–	–	–	–	–	GPIO_OUT(3:1)			RW	0x00
0x20	BBSMS	–	–	–	–	BBSEL(1:0)		BBSW	BBCHEN	RW	0x00
0x21	RTC_CTRL	–	–	–	EVERY(1:0)		MODE12_n24	RTC_AL_EN	RTC_EN	RW	0x00
0x22	RTC_UPDATE	–	–	–	–	UPDATE_TC(3:0)				W	0x00
0x23	RTC_SEC	–	SEC1(2:0)			SEC0(3:0)				RW	0x00
0x24	RTC_MIN	–	MIN1(2:0)			MIN0(3:0)				RW	0x00
0x25	RTC_HR	PM_nAM	–	HOUR1(1:0)		HOUR0(3:0)				RW	0x00
0x26	RTC_DAY	–	–	DAY1(1:0)		DAY0(3:0)				RW	0x01
0x27	RTC_MON	–	–	–	MONTH1	MONTH0(3:0)				RW	0x01
0x28	RTC_YR	YEAR1(3:0)				YEAR0(3:0)				RW	0x04
0x29	RTC_WKDAY	–	–	–	–	–	WEEKDAY(2:0)			RW	0x04
0x2A	RTC_AL_SEC	–	AL_SEC1(2:0)			AL_SEC0(3:0)				RW	0x00
0x2B	RTC_AL_MIN	–	AL_MIN1(2:0)			AL_MIN0(3:0)				RW	0x00
0x2C	RTC_AL_HR	AL_PM_nAM	–	AL_HOUR1(1:0)		AL_HOUR0(3:0)				RW	0x00
0x2D	RTC_AL_DAY	–	–	AL_DAY1(1:0)		AL_DAY0(3:0)				RW	0x01
0x2E	RTC_AL_MON	–	–	–	AL_MONTH1	AL_MONTH0(3:0)				RW	0x01
0x2F	RTC_AL_YR	AL_YEAR1(3:0)				AL_YEAR0(3:0)				RW	0x04
0x30	RTC_COMP_MSB	RTC_COMPH(7:0)								RW	0x00
0x31	RTC_COMP_LSB	RTC_COMPL(7:0)								RW	0x00
0x32	S1_PULL_EN	S1_APPCLKF_DLY(2:0)			S1_CMD_EN	S1_DAT3_EN	S1_DAT2_EN	S1_DAT1_EN	S1_DAT0_EN	RW	0x00
0x33	S1_PULL_DIR	–	–	–	S1_CMD_UP	S1_DAT3_UP	S1_DAT2_UP	S1_DAT1_UP	S1_DAT0_UP	RW	0x00

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Table 11−2. TWL92230 Register Map (Continued)

ADDRESS (HEX)	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	ACCESS TYPE	RESET (HEX)
0x34	S2_PULL_EN	S2_APPCLKF_DLY(2:0)			S2_CMD_EN	S2_DAT3_EN	S2_DAT2_EN	S2_DAT1_EN	S2_DAT0_EN	RW	0x00
0x35	S2_PULL_DIR	–	–	–	S2_CMD_UP	S2_DAT3_UP	S2_DAT2_UP	S2_DAT1_UP	S2_DAT0_UP	RW	0x00
0x36	MCT_CTRL1	–	APBUFDRV	S2BUFDRV	S1BUFDRV	S2_CMD_OD	S1_CMD_OD	S2CD_SWNO	S1CD_SWNO	RW	0x03
0x37	MCT_CTRL2	S2CD_DBEN	S1CD_DBEN	S2CD_BUFEN	S1CD_BUFEN	S2D1_BUFEN	S1D1_BUFEN	VS2_SEL(1:0)		RW	0xC0
0x38	MCT_CTRL3	–	–	–	–	S2_AUTO_EN	S1_AUTO_EN	SLOT2_EN	SLOT1_EN	RW	0x00
0x39	MCT_PIN_ST	–	–	–	–	S2_DAT1_ST	S1_DAT1_ST	S2_CD_ST	S1_CD_ST	R	0x00
0x3A	DEBOUNCE1	–	–	RESWARM_DB(5:0)						RW	0x05

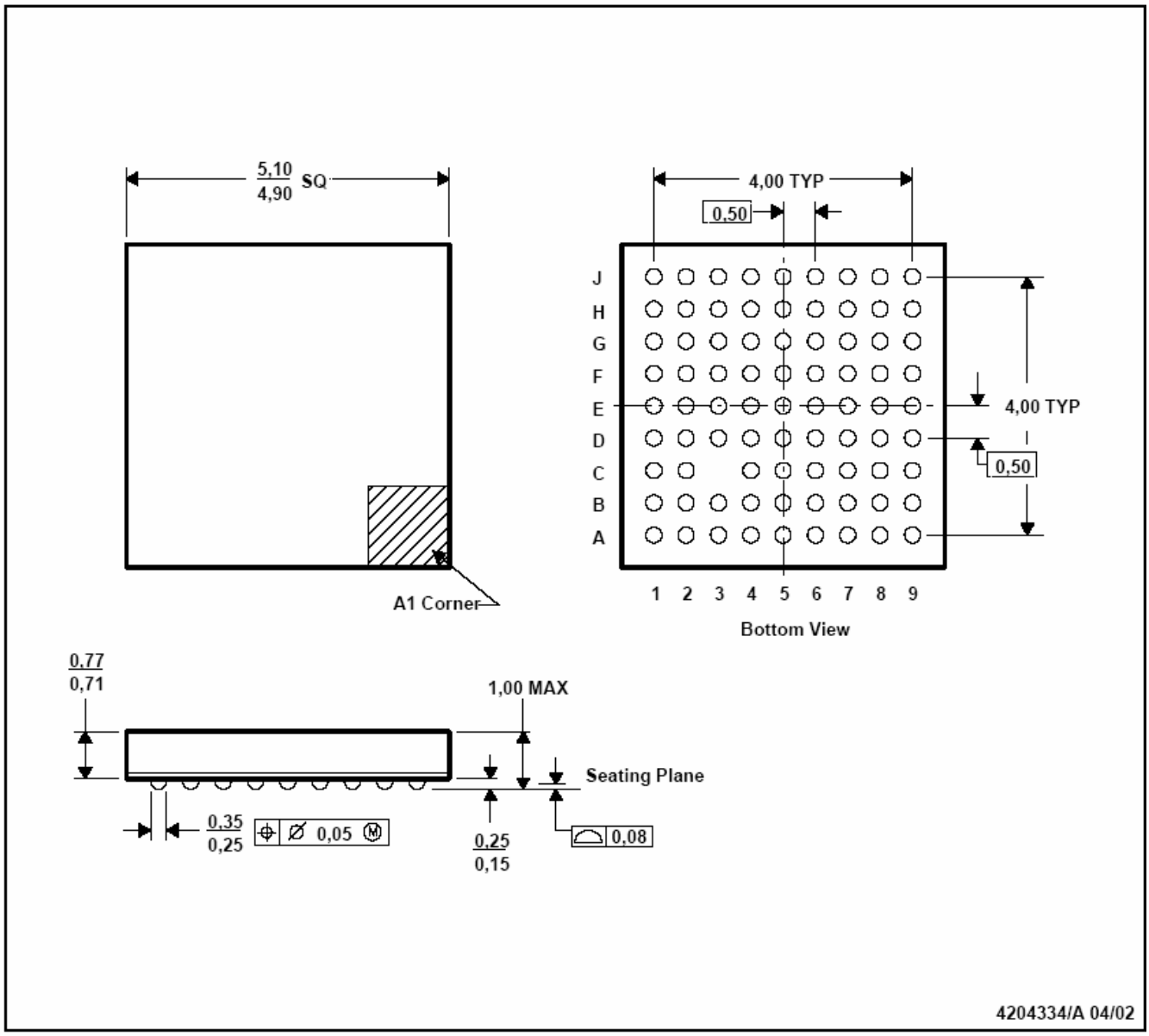
(1) Reset value for M_Config0/1/2 is 0x33. Reset value for M_Config3 is 0x31.
(2) Reset value for M_Config0/1/2 is 0x03. Reset value for M_Config3 is 0x00.
(3) Reset value for M_Config0/1/2 is 0x03. Reset value for M_Config3 is 0x00.
(4) UVLO_BYP or UVLO_EN depends on PG versions, see section 10.4, Table 10−5, and section 11.2.22 for details.

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12 Mechanical Information

12.1 Package Drawing and Dimensions

ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior BGA configuration.
D. Falls within JEDEC MO–225.
E. This package is lead–free.

Figure 12−1. TWL92230 Package Drawing (Bottom View)

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12.2 Ball Assignments/Locations

(April, 2005)

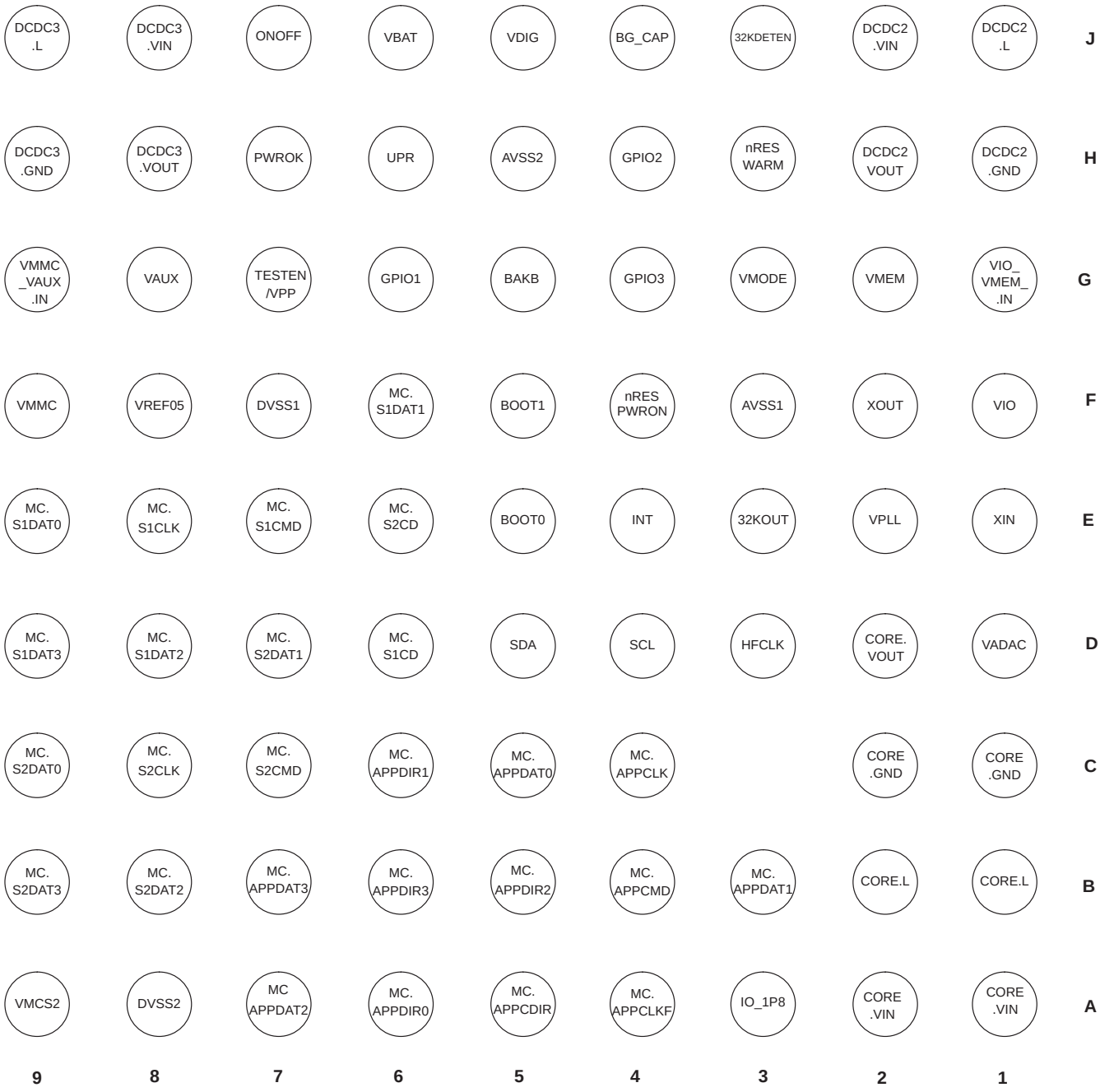


Figure 12−2. TWL92230 Ball Locations (Top View)

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12.3 Substrate Drawing and Pad Locations

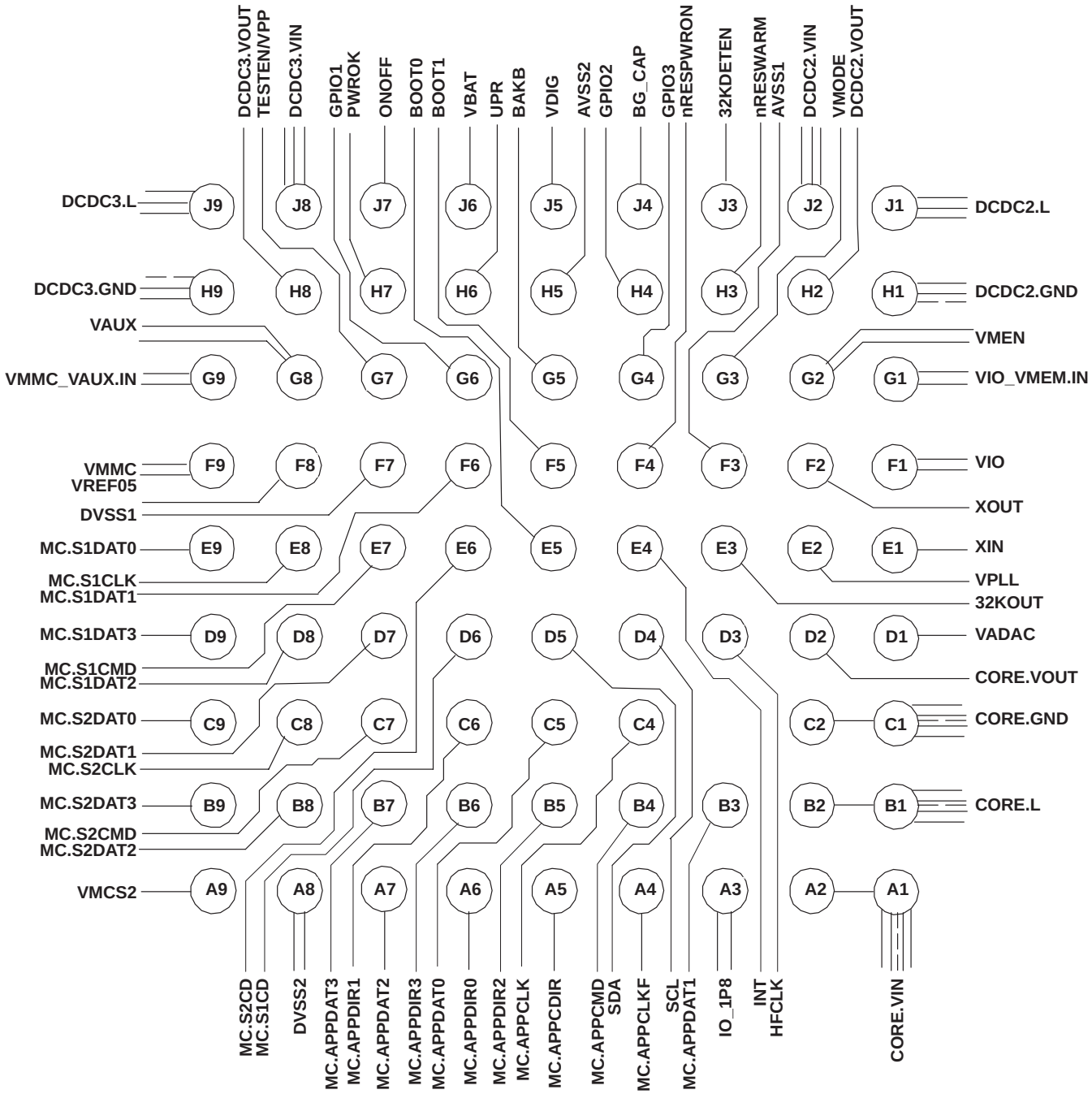


Figure 12−3. TWL92230 Substrate Drawing (Top View)

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12.4 Package Dissipation Rating

TWL92230 maximum power dissipation can be calculated using this formula:

$$\text{Power Rating} = \frac{T_J \text{ (junction temperature)} - T_A \text{ (ambient temperature)}}{\text{Derating Factor } (\theta_{JA} \text{ or } \theta_{JB})}$$

Table 12−1 shows the TWL92230 Package Power Ratings.

Table 12−1. TWL92230 Package Power Ratings

DERATING FACTOR (mW/°C)	POWER RATING T_A = 20°C (W)	POWER RATING T_A = 60°C (W)	POWER RATING T_A = 85°C (W)
θ_{JA} (Junction to ambient) = 57	1.9	1.2	0.7
θ_{JB} (Junction to board) = 40	3.1	1.9	1.2

Assumptions:

1. JEDEC High−K board
2. 0 lfm (linear feet per minute) airflow
3. Junction temperature = 125◦C
4. Ambient temperature = 85◦C
5. VBAT = 4.2 V

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13 Appendix A—Digital Voltage Scaling Implementation

The VCORE regulator voltage setting can be controlled directly through the I2C interface or by means of an external pin, VMODE. The selection of control is made through the I2C bit, HW_nSW, in the VCORE_CTRL1 register.

In general, when HW_nSW=0 (reset value), the VCORE voltage setting is determined by the VCORE_VOLT bits found in the VCORE_CTRL1 register. When HW_nSW=1, the VCORE voltage setting is controlled by the DVS (Digital Voltage Scaling) state-machine, and is determined by the ROOF and FLOOR bits found in the VCORE_CTRL4 and VCORE_CTRL3 registers, respectively, and the state of the pin VMODE:

- VMODE = 1, VCORE output voltage is set to ROOF.
- VMODE = 0, VCORE output voltage is set to FLOOR.

Furthermore, when HW_nSW=1, the VCORE output voltage transitions between ROOF and FLOOR can be made in a single jump or multiple steps. The selection of control is made through the I2C bit, STEP_nJMP, in the VCORE_CTRL1 register:

- STEP_nJMP = 1, the VCORE output voltage steps between ROOF and FLOOR.
- STEP_nJMP = 0, the VCORE output voltage jumps between ROOF and FLOOR.

For VCORE electrical characteristics, see section 3.1.
For additional VCORE Scaling Implementation, see section 10.1.3.

13.1 Setup

13.1.1 Software Control (HW_nSW = 0)

For software control, no special setup is required. To change the output voltage of the VCORE regulator, write to the VCORE_VOLT bits in the VCORE_CTRL1 register. The HW_nSW bit in the VCORE_CTRL1 register should remain 0.

13.1.2 Hardware Control (HW_nSW = 1)

For hardware control, care must be taken when setting up registers to ensure desired behavior. Depending on the state of VMODE at the time HW_nSW is written from a 0 to a 1, the voltage setting for VCORE will begin to transition to ROOF (VMODE=1) or FLOOR (VMODE=0). If STEP_nJMP=0, that transition will occur as one single jump. If STEP_nJMP=1, the transition will occur as multiple steps. Therefore it is important that ROOF, FLOOR and VMODE be setup properly before HW_nSW is written from a 0 to a 1. Since STEP_nJMP is in the same register as HW_nSW, it may be desirable and it is permissible to be set at the same time that HW_nSW is written from a 0 to a 1.

13.2 Transitioning from ROOF to FLOOR

13.2.1 The PWROK Signal

During the time when the VCORE voltage setting is transitioning between ROOF and FLOOR, the PWROK pin is brought low by the DVS logic to indicate the VCORE output voltage is not yet at the desired level.

PWROK comparator is disabled with its output pulled high during sleep mode.

PWROK is functional only during voltage scaling.

13.2.1.1 The BYP_COMP Bit

The above statement holds true even if the BYP_COMP bit is set to 1. To gain a better understanding of the effect of the setting of the BYP_COMP bit on the behavior of the DVS, see Figure 13−1 which depicts the implementation of the bypassing mechanism.

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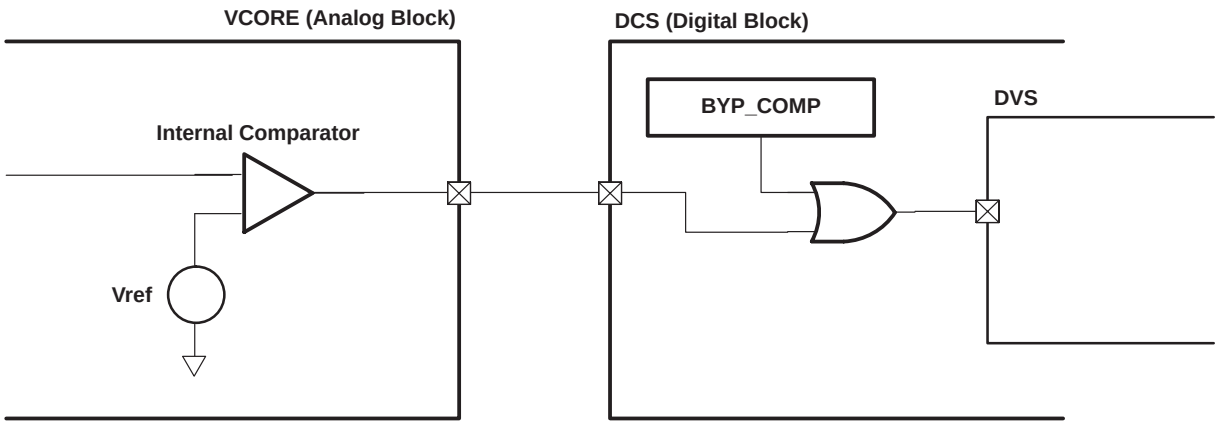


Figure 13−1. Bypassing Mechanism

It can be noted that the effect of the BYP_COMP bit when STEP_nJMP=1 will only be seen if the time between steps is smaller than the time required for the VCORE voltage to come into range (see case 2 in section 13.2.1.2). It can also be noted that the effect of the BYP_COMP bit when STEP_nJMP=0 is usually (depending on the ROOF and FLOOR settings) more evident and can have a greater affect on the DVS behavior and the time that the PWROK pin is held low.

13.2.1.2 STEP_nJMP = 1

When STEP_nJMP=1, PWROK is held low during the entire transition even if the internal VCORE comparator signal indicates the voltage is within an acceptable range. This is needed as the individual step sizes are smaller than the tolerance specified for the regulator (see diagram below), hence the VCORE comparator signal may never go low. If the output voltage falls out of range during the transition, the output of the internal comparator will be deasserted (low voltage level) and the step sequence halted (even if the STEP_PER timer has expired) until the regulator comes back into range. This will in effect override the STEP_PER setting, which is the time between steps.

In the example below, the output of the VCORE voltage regulator is stepping between FLOOR = 00000 (1.000 V) and ROOF = 00111 (1.175 V). Four different ramp profiles are shown, resulting in 2 different cases of behavior of the DVS.

Case 1 shows the behavior of the DVS for the VCORE output voltage ramps with slopes 1, 2 and 3 and with BYP_COMP = 0. In this scenario, the VCORE output voltage will always be within the specified range of −4.7% to +5%. Therefore, the time between steps is determined by the equation

t_{PER} = STEP_PER $\times$ 10 µs + 3.33 µs (typical)

After the last step and once the VCORE comparator signal indicates the output is within range, the PWROK pin is held low an additional period of time to allow the regulator to settle. This time is determined by the equation

t_{STL} = STEP_PER $\times$ 10 µs + 1.67 µs (typical)

In this case, the DVS behavior and PWROK pin timing would have been the same for the setting of BYP_COMP = 1. This is because the internal comparator never went low.

Case 2 shows the behavior of the DVS for the VCORE output voltage ramp with slope 4 and with BYP_COMP = 0. In this scenario, the VCORE output voltage falls out of range (at the 4^{th}, 5^{th}, 6^{th}, and 7^{th} step), resulting in the deassertion (low voltage level) of the VCORE comparator signal. If the VCORE output voltage comes back into range within the time t_{PER} after the step (at the 5^{th} and 6^{th} step), then the DVS behaves normally. However, if the VCORE output voltage does not come back into range within the time t_{PER} after the step (at the 7^{th} step) then the DVS state machine is halted until the output voltage is again within range. After the last step and once the VCORE comparator signal indicates the output is within range, the PWROK pin is held low an additional amount of time, t_{STL} (see above equation).

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In this case, the DVS behavior and the PWROK pin timing would have been affected for the setting of BYP_COMP = 1. Namely, t_{EXT1} and t_{EXT2} would have been 0 as the gated comparator signal would have indicated that the voltage was within range. This would have resulted in the same DVS behavior as in case 1, although it should be clear that the PWROK pin would have been set to 1 before the VCORE voltage was within tolerance.

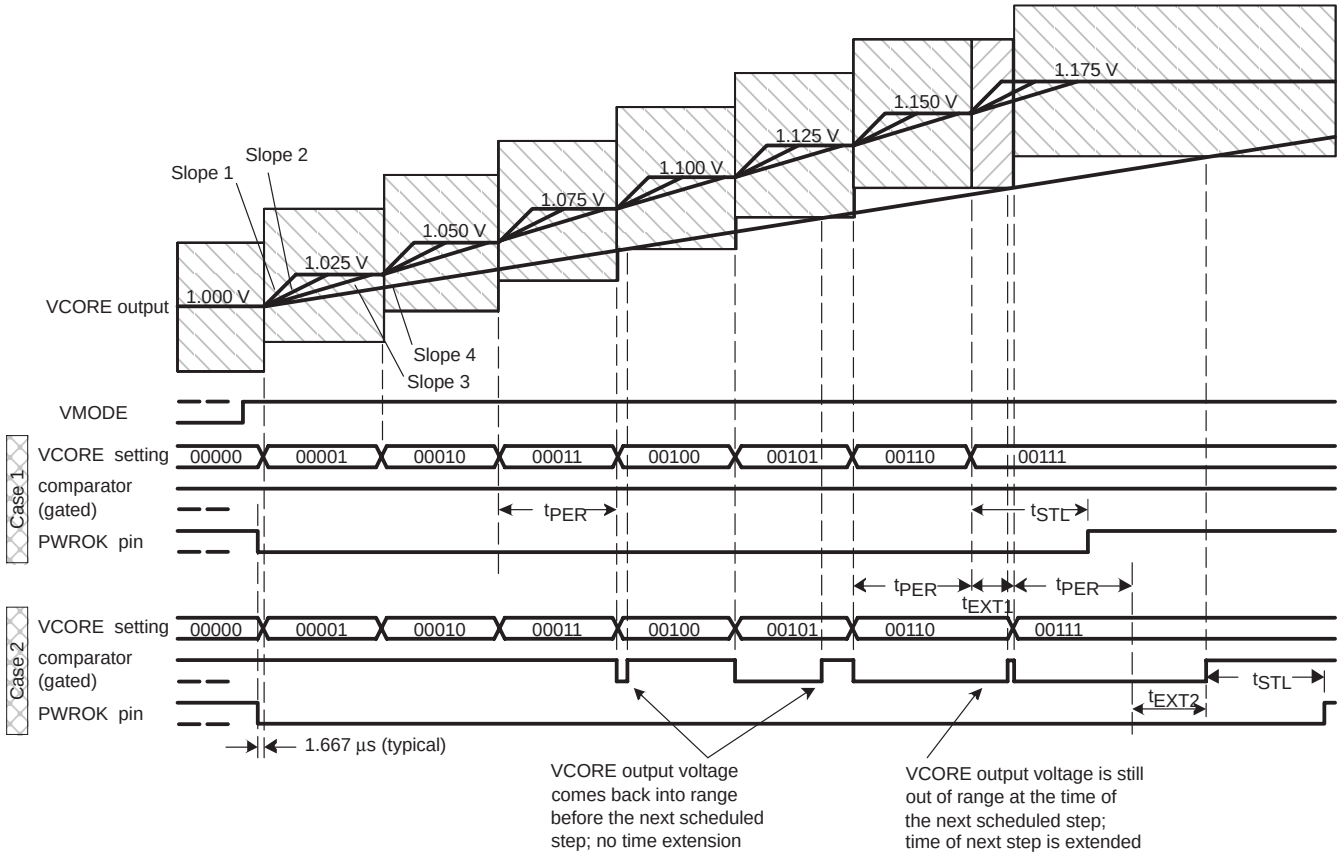


Figure 13−2. VCORE Case 1 and Case 2

13.2.1.3 STEP_nJMP = 0

When STEP_nJMP=0, the PWROK pin is immediately brought low by the DVS logic regardless of the state of the VCORE comparator signal or the setting of the BYP_COMP bit. Then, depending on the setting of BYP_COMP and the behavior of the VCORE comparator signal, the PWROK pin is then held low an additional programmable time period indicated by STEP_PER plus a small amount of time for the DVS state machine to transition through various states. Part of this extra time is required at the beginning of the DVS state machine's sequence, and will be referred to as t_{SM1}. The time t_{SM1} is always 10 µs (typical), but may be absorbed into the time that the VCORE comparator is low (this will be discussed later). The remaining portion of the extra time is required at the end of the DVS state machine's sequence and will be referred to as t_{SM2}. The time t_{SM2} is always 6.67 µs (typical) and will always be included in the equation for the length of time that the PWROK pin is held low.

When BYP_COMP=1 the total time that the PWROK pin will be held low can be described by the following equation

$t_{PER} = t_{SM1} + STEP_PER \times 10\ \mu s + t_{SM2}$
where t_{SM1} = 10 µs and t_{SM2} = 6.67 µs (typical)

When BYP_COMP = 0, the DVS logic uses the VCORE comparator signal and waits for it to indicate that the voltage is good. The time that the VCORE comparator signal is low will be referred to as t_{CMP}. So the total time that the PWROK pin is held low can be described by the following equations.

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$t_{PER} = t_{CMP} + STEP_PER \times 10\ \mu s + t_{SM2}$
when $t_{CMP} \geq 10\ \mu s$, where $t_{SM2} = 6.67\ \mu s$ (typical)

$t_{PER} = t_{SM1} + STEP_PER \times 10\ \mu s + t_{SM2}$
when $t_{CMP} < 10\ \mu s$, where $t_{SM1} + t_{SM2} = 16.67\ \mu s$ (typical)

Notice that the second equation is the same as the equation for the case of BYP_COMP=1.

Figure 13−3 shows the DVS behavior and PWROK pin timing for the case when either the VCORE comparator signal never goes low or goes low for a short time. It should be noted that the DVS behavior and the PWROK pin timing would be unaffected by the BYP_COMP setting.

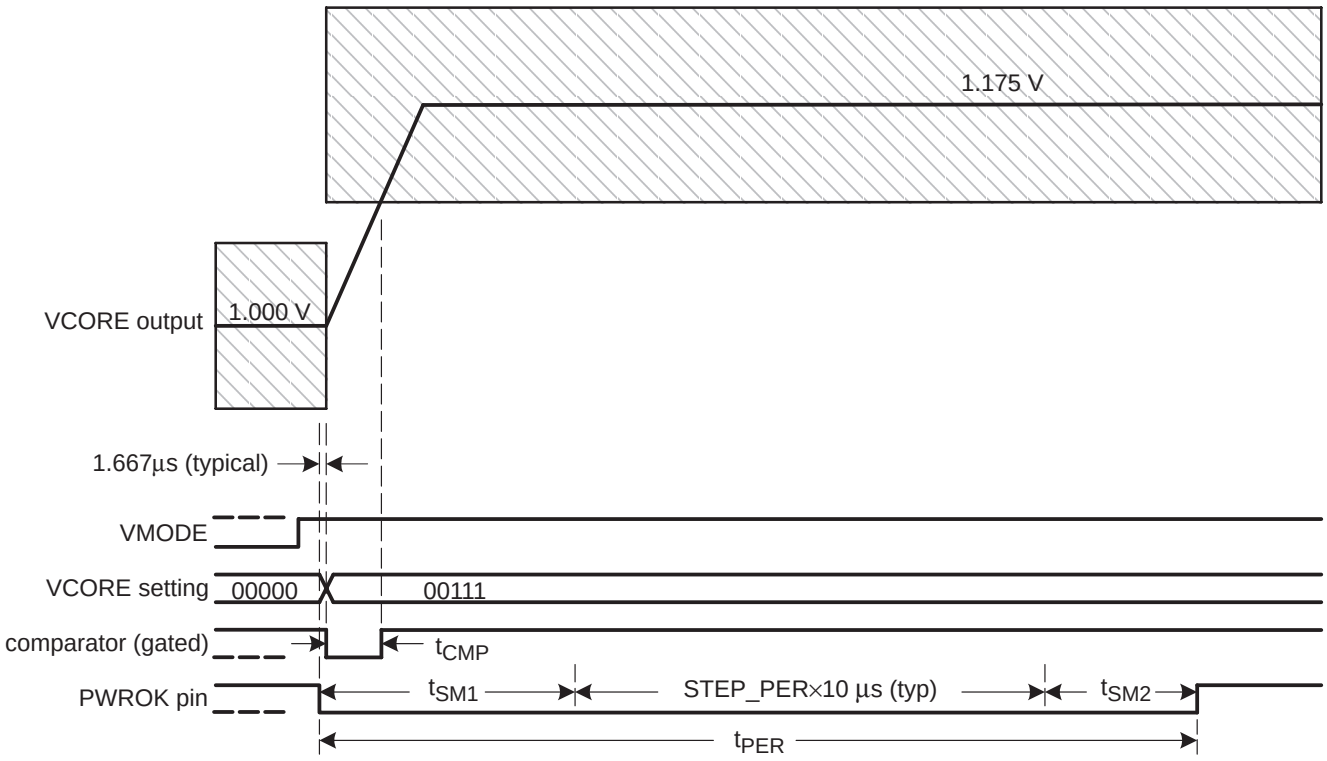


Figure 13−3. DVS Behavior and PWROK Pin Timing

Figure 13−4 shows the DVS behavior and PWROK pin timing for the case when BYP_COMP = 0 and the VCORE comparator signal goes low for more than 10 µs (typical). It should be noted that for a setting of BYP_COMP = 1, the parameter t_{CMP} would be 0 and the second equation would be used.

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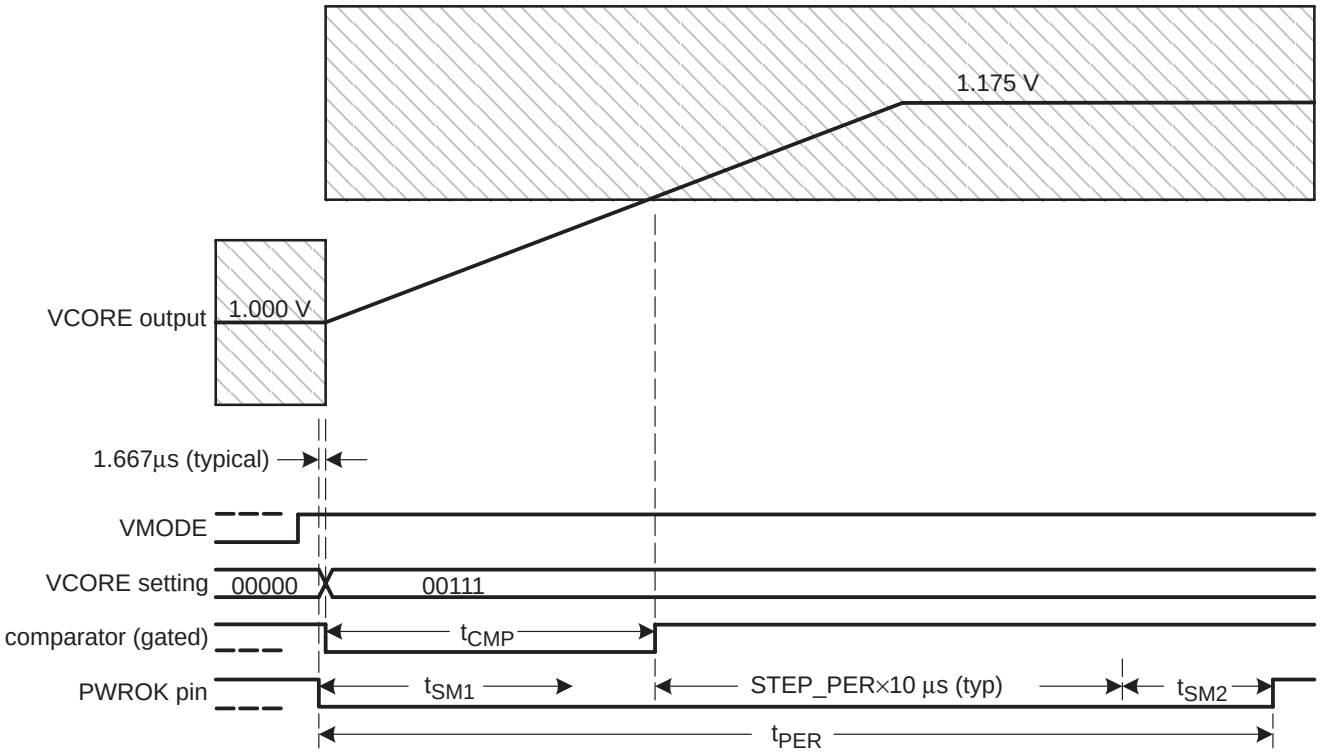


Figure 13−4. DVS Behavior and PWROK Pin Timing BYP_COMP=0

13.2.2 ROOF, FLOOR, STEP_nJMP, and HW_nSW Settings

During a transition (while the DVS state-machine is running) no changes will be recognized by the DVS in any of the I2C bit settings VCORE_VOLT, ROOF, FLOOR, HW_nSW, or STEP_nJMP. After the transition has completed, the new I2C register settings will take affect.

When HW_nSW = 1, VMODE determines whether or not the target voltage setting is ROOF (VMODE=1) or FLOOR (VMODE = 0). There is no limitation on the relative settings of ROOF and FLOOR, that is, ROOF may be less than FLOOR.

13.2.3 Initiating a Transition

There are three mechanisms by which a transition may be initiated. The following paragraphs describe those mechanisms.

13.2.3.1 HW_nSW Is Written From 0 to 1 Through I2C

When HW_nSW goes from 0 to 1, the DVS state-machine is started and (depending on the state of STEP_nJMP) begins to transition to the target setting; ROOF if VMODE = 1 or FLOOR if VMODE = 0. If the VCORE_VOLT setting already equals the target setting, the PWROK signal will not go low and the state-machine remains in the idle state.

13.2.3.2 HW_nSW Is Written From 1 to 0 Through I2C

When HW_nSW goes from a 1 to a 0, the I2C bits VCORE_VOLT setting immediately becomes the VCORE regulator setting. The STEP_nJMP bit has no effect on the transition (a single jump from current setting to VCORE_VOLT). Furthermore, PWROK does not go low. If the state-machine was in the middle of a transition, the write to HW_nSW is not recognized until the DVS state-machine has finished. After the DVS state-machine has finished, the new value of HW_nSW will immediately take effect. Note: If VCORE_VOLT is equal to the current setting (ROOF or FLOOR), from a system point of view, nothing happens.

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13.2.3.3 VMODE Is Toggled

When VMODE is toggled (HW_nSW=1), a transition will begin if the current setting does not equal the target setting, that is, if ROOF does not equal FLOOR. If VMODE toggles during a transition, the new value of VMODE is not recognized until the current transition has been completed. After the transition has completed, the new value of VMODE will immediately take effect.

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14 Appendix B—Parameter Definitions

Below are the definitions of parameters used in this design specification document. They are valid over process, voltage, and temperature, unless otherwise stated.

Load Regulation

The percentage change in output voltage due to a change in output loading over a specified range. This is usually a measurement of the output deviation as the loading is changed from no load to full load, but with input line, temperature, etc. remaining constant.

Line Regulation

The percentage change in output voltage due to a change in input voltage level. This is usually a measurement of the output deviation as the input voltage is varied from low line to high line. The percentage change in output voltage caused by varying the input voltage over a specified range, with output load, temperature, etc., remaining constant.

Transient Response

The response of a circuit to a sudden change in an input or output quantity. In power supplies, this is the excursion of the output voltage (due to the transient) and the time it takes to recover from a step change in the output load (Transient Load Regulation) or the input voltage (Transient Line Regulation). It does not include the excursion due to the DC variation.

Output Voltage Accuracy

The maximum allowable deviation of the DC output of a converter from its ideal or nominal value, due to process, voltage, temperature and load current. It does not include Transient Response unless stated otherwise. It's typically expressed as a percentage of output voltage.

Inrush Current

The maximum, instantaneous input current as measured during the initial turn−on of the power supply. This current reduces to a lower steady−state current once the input capacitors charge. Also called input surge current. It is typically the charging current of the input capacitance.

Soft start

A feature that ensures the smooth, controlled rise of the output voltage. This feature protects the switching transistors and other devices from transients when the power supply is turned on.

Short−circuit current

The output current limit value of the power supply that prevents damage to the power supply and the system caused by short circuits in which is used.

PSRR

Power Supply Rejection Rate. It's typically expressed in dB and within a specified frequency range, for a given input voltage.

Conversion Efficiency

The ratio of total output power to input power expressed as a percentage. Derived by the equation:

Efficiency(%) = (Output Power/Input Power) * 100

Efficiency is normally measured at a specific output power (output load current) and nominal input line conditions.

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ESR

Equivalent Series Resistance. The resistance in series with an ideal capacitor. ESR sources include lead resistance, terminal losses of the capacitor, etc., but it does not include external parasitic resistances such as bondwires and lead resistance of devices connected to the capacitor.

Overshoot

A transient change in output voltage that exceeds specified accuracy limits. Typically occurs on the power supply turn on/off or with a step change in output load or input line. It's typically expressed as a percentage of the settled output voltage.

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TWL92230CZQE	PREVIEW	BGA MICROSTAR JUNIOR	ZQE	80		Pb-Free (RoHS)	SNAGCU	Level-3-255C-168 HR
TWL92230CZQER	PREVIEW	BGA MICROSTAR JUNIOR	ZQE	80		Pb-Free (RoHS)	SNAGCU	Level-3-255C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

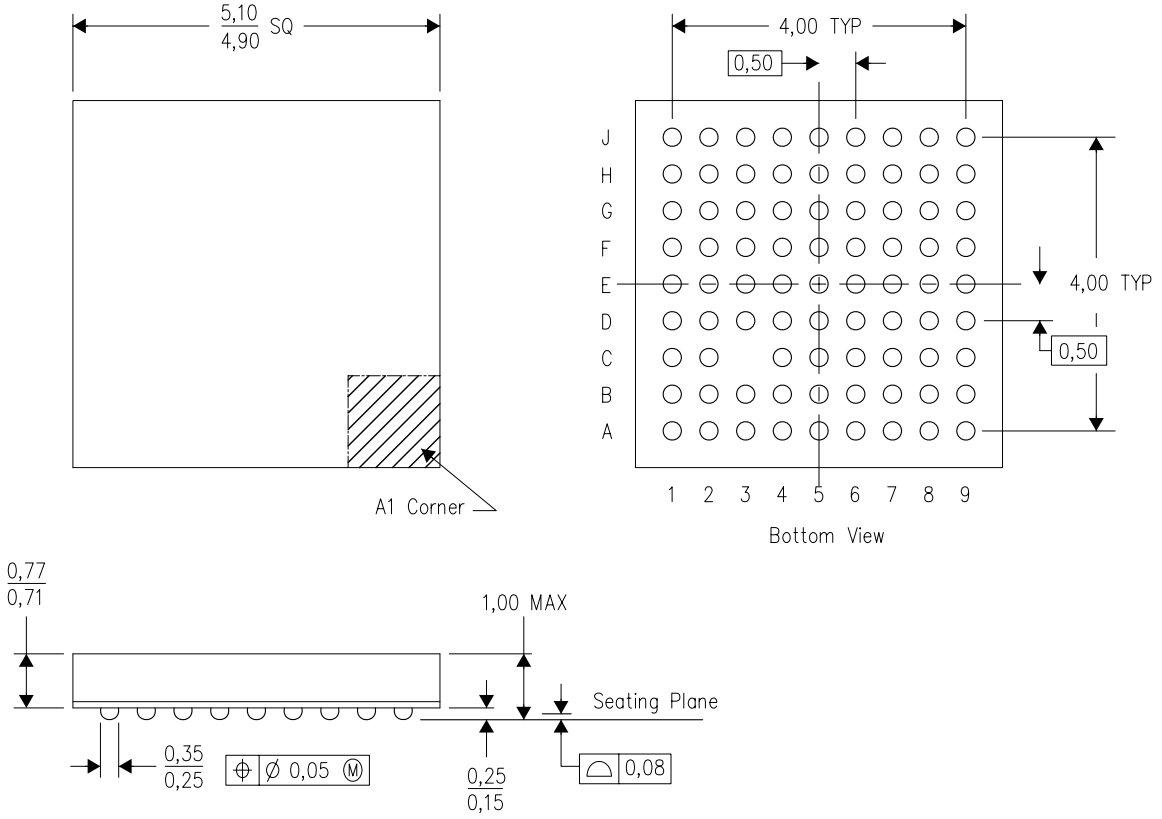
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



4204334–6/F 07/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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