Prabhjot Kaur
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OBJECTIVE

Seeking Internship/Co-op opportunities to utilize ASIC/VLSI/Digital Design, SoC Design and Digital Design Verification skills and knowledge or opportunities such as Technical, Non-Technical, System/Data Analyst or Application Engineer.

EDUCATION

M.S. in Electrical Engineering (GPA: 3.53/4)   **May 2018**
San Jose State University, San Jose, CA
B.E. in Electronics and Communication Engineering (GPA: 7.12/10)   **June 2015**
Thapar University, Punjab, India

RELATED COURSEWORK: ASIC CMOS Design, Digital System Design, Principal of Semiconductors, SOC Design, Design System Verification, Technical Writing, HI-Speed CMOS Circuits, Advanced Computer Architecture, Digital Design for DSP and AI/DNN.

PROJECTS

LOOK BACK COMPRESSOR, SJSU, Oct-Nov 2017
- Collaborated with a team of two to design and debug a compressor that receives data one byte at a time and places it in memory. It outputs the results by looking back in the stream for a piece of data the same as the data contained in the current position going forward.
- Utilized Verilog Skills, ASIC CMOS Designs and concept of pipelining, synthesizable code guidelines and timing constraints.
- Executed scheduled meetings with team member, strategized and analyzed the project as well as polished technical skills and concepts and succeeded to design working compressor.
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FLOATING POINT ADDER MULTIPLIER USING FIFO, SJSU, September 2017
- Designed FIFO and implemented with floating point adder multiplier to synthesize at 250MHz.
- Created a FIFO, implemented pipelining concepts and manage data flow between adder and multiplier.
- Demonstrated knowledge of Digital Design, Verilog skills and improved functionality of a simple design.

TRANSMISSION GATE LOGIC BASED 32:1 MUX CIRCUIT USING CADENCE, SJSU, March-May 2017
- Designed a mux using transmission gates using Cadence Virtuoso.
- Solidified Hi-Speed CMOS concepts and utilized it to create a design using Cadence.
- Delivered results to demonstrate functionality and efficiency of Transmission gate based MUX.
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FPGA COMPATIBLE CNN CODE, SJSU, Fall 2017
- Computed a neural network that is compatible of FPGA Board.
- Drafted design code in Verilog from provided MATLAB code.
- Succeeded in understanding functionality of Altera FPGA Board and CNN concepts.

SKILLS: Cadence Virtuoso, MATLAB, C, Python, VHDL, Verilog, Assembly Language, ModelSim, QuestaSim, VCS, Design Vision, Windows, IOS, NCSim, System Verilog, OVM/UVM.

ACTIVITIES

OFFICE AID, International House, SJSU, 2018-Present
- Maintaining and documenting monetary transactions.
- Attending phone calls, organizing meetings and marketing upcoming events.

IEEE (Institute of Electrical and Electronic Engineers) Member, 2017-Present
CFO/Student Council, International House, SJSU, 2016
- Collaborated with team of 7 student council members via weekly meetings to discuss expenses, upcoming events and strategizing and updating members via Power Point presentation and Spreadsheets.