Sunny Desai

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Summary:

- Enthusiastic, highly-motivated Electrical Engineer with proven leadership capabilities.
- Strong experience in using EDA tool Synopsys VCS for simulation.
- Strong experience in using Synopsys Design Compiler for synthesis of RTL code.
- Having an expertise in ASIC designing and SOC verification
- Strong understanding of ASIC design flow from specifications to Place and Route.
- Strong understanding of FPGA design cycle.
- Expertise in developing RTL design using Verilog and system Verilog languages.
- Expertise in building Digital Logic Design.
- Expertise in developing testing environment using UVM testbench.

Experience:

Product Design Intern — Scirobot — March'17 - June'17

- Monitored and produced partial designs from concept to production.
- Programmed Raspberry Pi using PYTHON for interfacing of different sensors.
- Designed a circuit with raspberry pi interfaced with heart rate sensor, GSR sensor, IMU sensor and LED.
- Resolved all aspects of product design activities starting at early stages of the concept design, into prototyping and manufacturing on PD team.
- Advocated for Alzheimer's disease curability through non-pharmacological methods with the assistance of UCSF's research team.
- Determined the problem, identified the audience and vision behind the product and used goal setting to achieve my outputs using solid works.
- Visited elderly living homes and conducted customer satisfaction surveys.

Academic Projects — Jan'16 – Dec' 17

1. **Verification of DDR3 memory controller using UVM.** Fall'17
   - Using CAN controller as master and DDR3 memory controller as a slave.
   - Designing the Reference Model.
   - Generating Test Cases and Test bench for verifying CAN transmitter and initializing DDR3 memory controller.
   - Developed Cross Domain Clocking block using Asynchronous FIFO.
   - Verifying the Read/Write operations of the memory controller.
2. **Designed a synthesizable Verilog RTL code for CAN-BUS transmitter on AHB bus.** Spring'17
   - Fragmented input chunks of data into different Frames.
   - Developed AHB bus module working on 100 MHz frequency.
   - Validated the frames by implementing a CRC checker.
   - Interfaced the transmitter on AMBA-AHB bus protocol.
   - Designed Bandwidth Arbitrator.
3. **Designed and synthesized Source Routed Network Switch in Verilog RTL language.** Fall'16
   - Implementing CRC checker for validating packet.
   - 32 input ports and 32 output ports with 64 bytes 64 FIFO and 256 KB main memory.
4. **Designed and simulated FIR filter on an FPGA in Altera Quartus Prime software**. Fall'16
5. **Designed LMS adaptive Filter on Altera Quartus Prime software.** Fall'16
6. **Successfully designed a subset of Altera Nios II instruction set architecture in Xilinx.** Summer'16
   - Pipelined structure of NIOS II architecture.
   - Detection and solving different pipelining hazards.
   - Developed write and instruction memories.
   - Video presentation of the RTL simulation.
7. **Designed n-bit sequential and array binary multipliers using conditional sum adders.** Spring'16

Mathematics Tutor **San Jose State University** **Jan'17 – Dec' 17**

- Help students in understanding the concepts they failed to understand during class.
- Prepare students for the upcoming exams.
- Tutor for subjects like college algebra, calculus for business, math probability and statistics, linear algebra and differential equations, and some more.

Instructional Student Assistant **San Jose State University** **July'16 – Dec' 16**

- Instructional Student Assistant and Grader for the undergraduate level course of 'Digital Logic Design'.
- Collaborated with professor to develop a weighted grading system.
- Reviewed assignments and evaluated students' coursework.
- Modulated online records and assisted professor in developing lecture notes.
- Held office hours on a weekly basis and resolved students' doubts.

Technical skill:

• EDA/CAD/Software tools	Cadence design compiler, Xilinx ISE, Xilinx Vivado, Altera Quartus, Synopsys VCS.
• Programming Languages	Verilog, SystemVerilog, UVM, C.
• Bus Protocols	APB, AHB, I2C, SPI.
• Scripting Language	Python.
• Others	RTL design and simulation, gate level synthesis, PCB designing, FPGA design flow, Place and Route, Design for Test(DFT), BIST, SCAN, DSP designing, Static timing analysis, ASIC design flow, computer architecture, ASIC verification, UVM methodology.

Education:

M.S, Electrical Engineering — GPA: 3.64
San Jose State University, California

B.E, Electronics and Communication Engineering — GPA: 3.60
Gujarat Technological University, India

Courses:

- **Spring 2017:** EE272- SoC Design and Verification with System Verilog, EE281- Internetworking.
- **Fall 2016:** EE287- ASIC CMOS Design, EE278- Digital Design for DSP/ Communications.
- **Summer 2016:** EE275- Advanced Computer Architectures.
- **Spring 2016:** EE271- Digital System Design and Synthesis, EE221- Semiconductor Devices I, EE210- Linear System Theory

Activities:

- Managing committee member of Indian Student Organization at San Jose State University.
- Represented city at state level karate championship.
- Silver medalist of intercity karate championship.
- Brown-senior belt in karate.