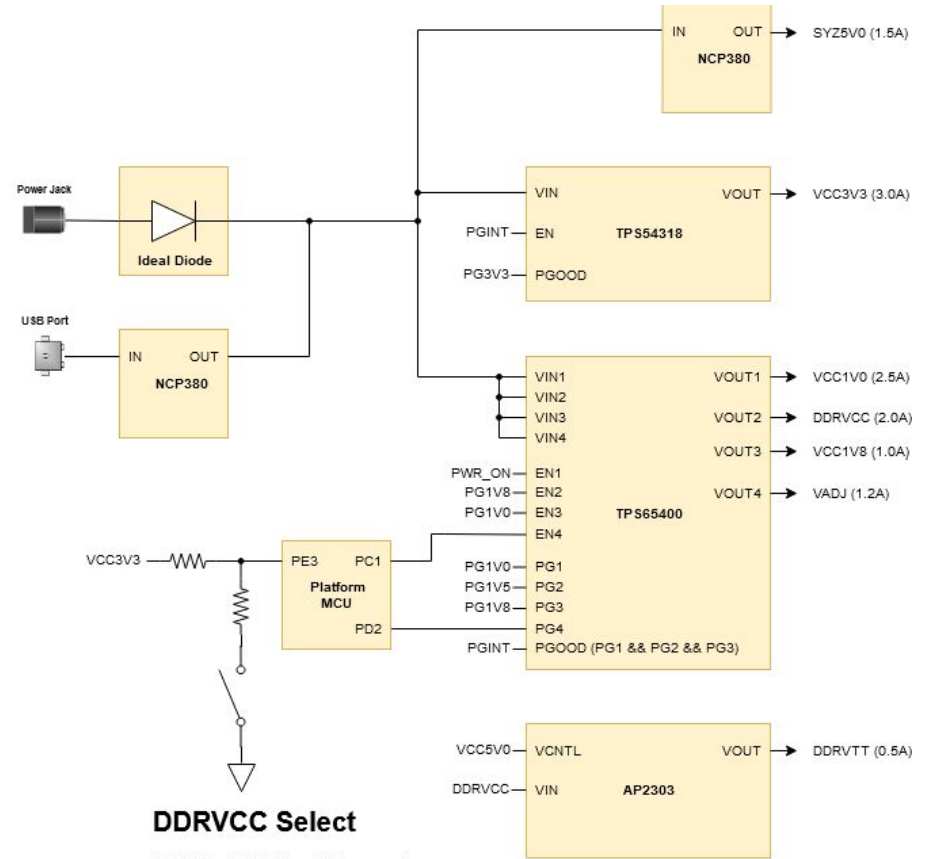


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- 2 IO, Pmods and Zmods
- 3 USB Hub
- 4 USB FIFO/SPI
- 5 Configuration
- 6 FPGA Banks
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- 9 DDR3 Memory
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- 11 Power Regulation
- 12 Power regulation
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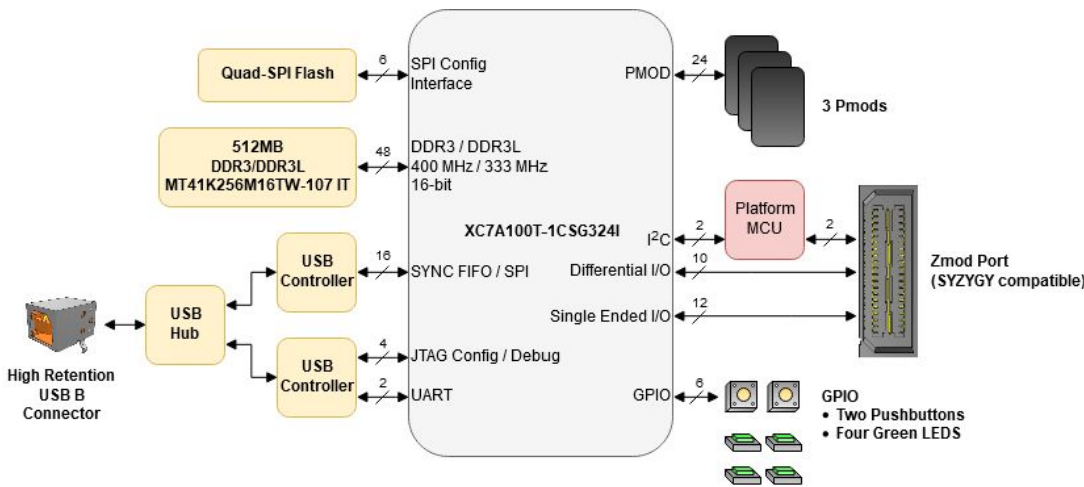
Power Tree



DDRVCC Select

DDRVCC = 1.35V with switch in on position
 DDRVCC = 1.5V with switch in off position

Block Diagram

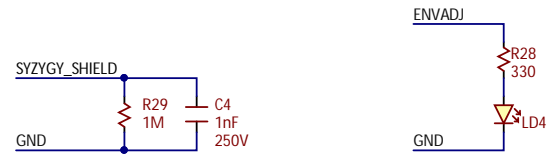
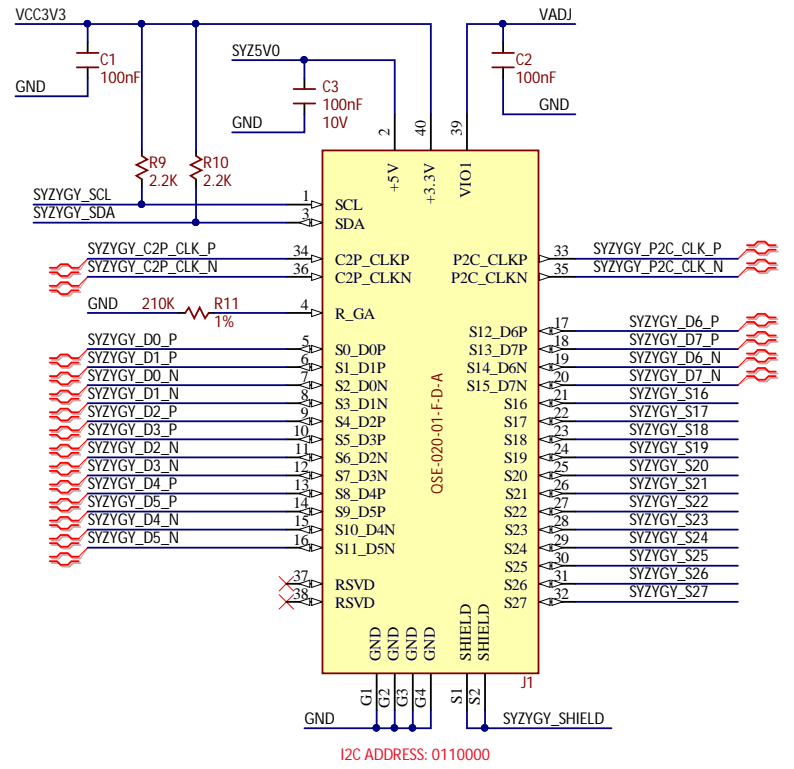
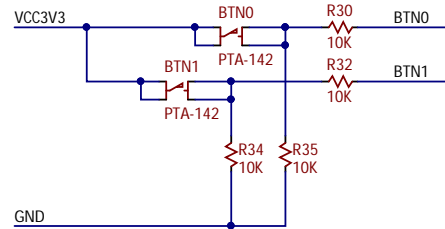
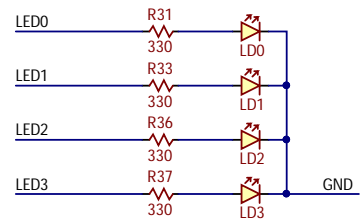
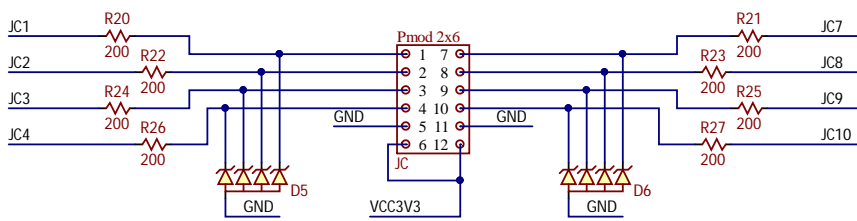
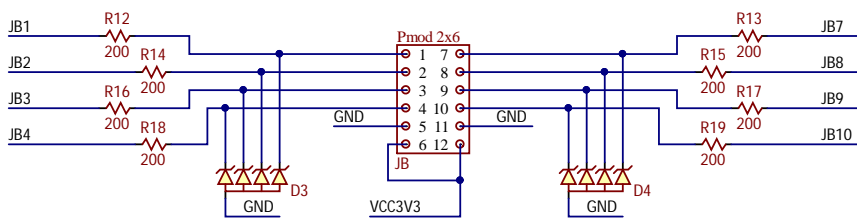
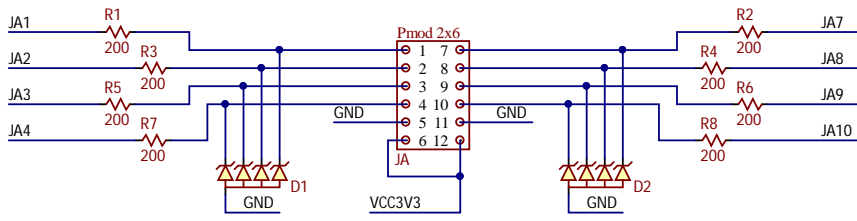


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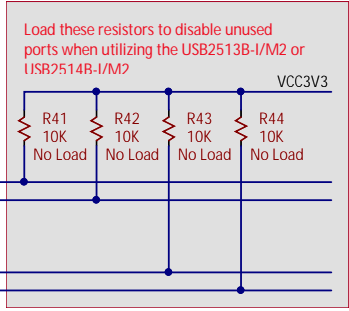
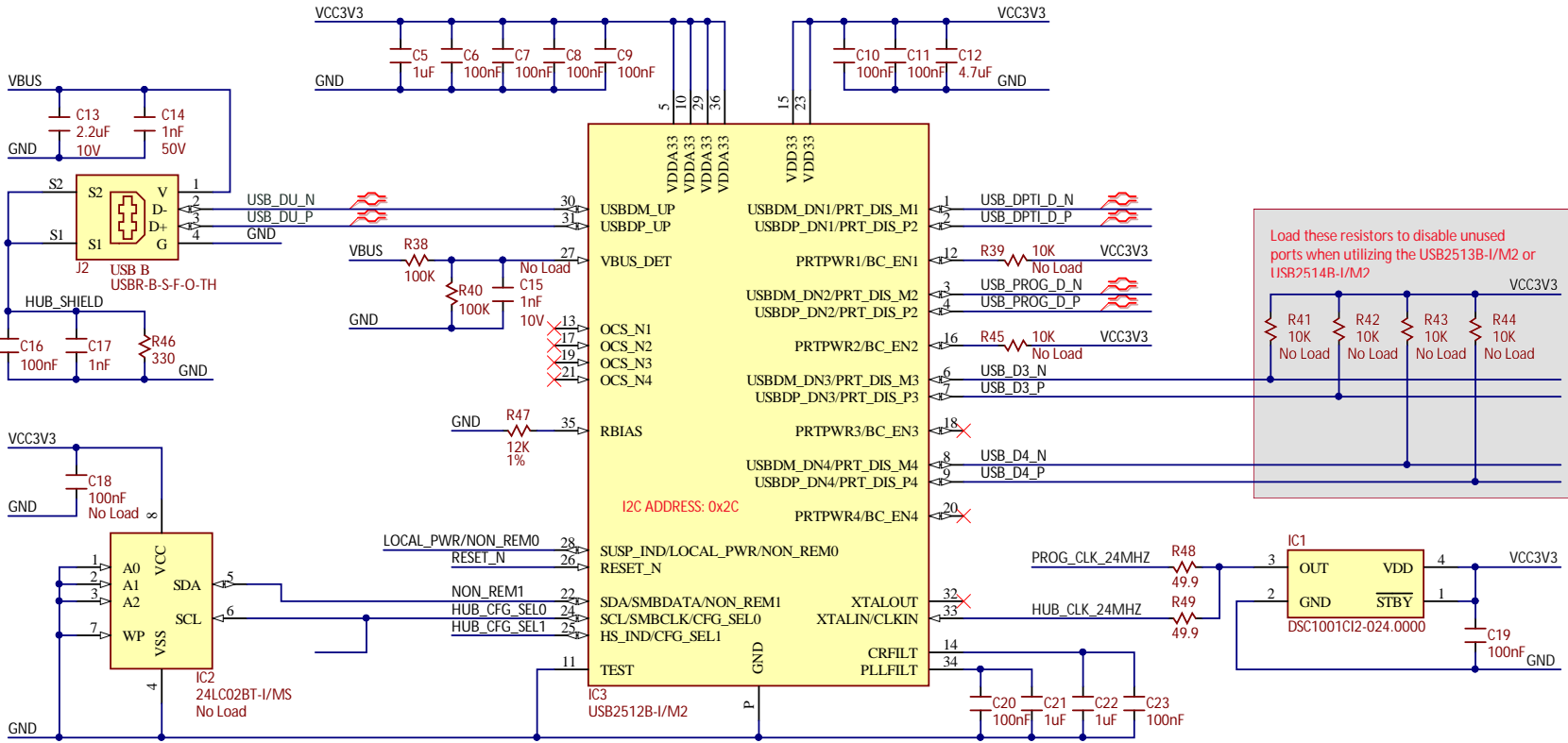




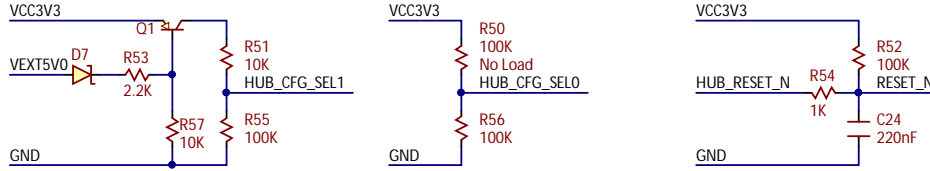
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Foot F1 Foot F2 Foot F3 Foot F4

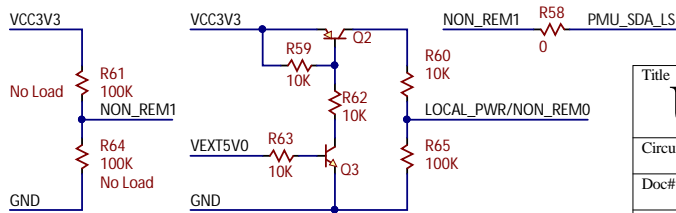


CFG_SEL1	CFG_SELO	Hub Configuration
0	0	Default Configuration, Strapping Enabled, Self Powered
0	1	Configured via SMBus, Strapping disabled
1	0	Default Configuration, Strapping Enabled, Bus Powered
1	1	Configured via I2C EEPROM, Strapping disabled



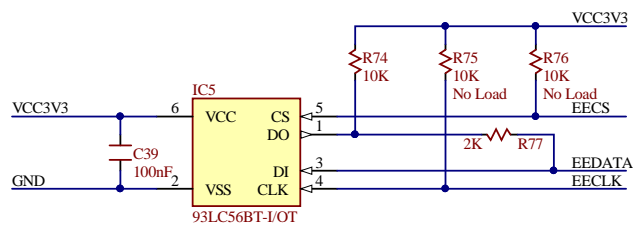
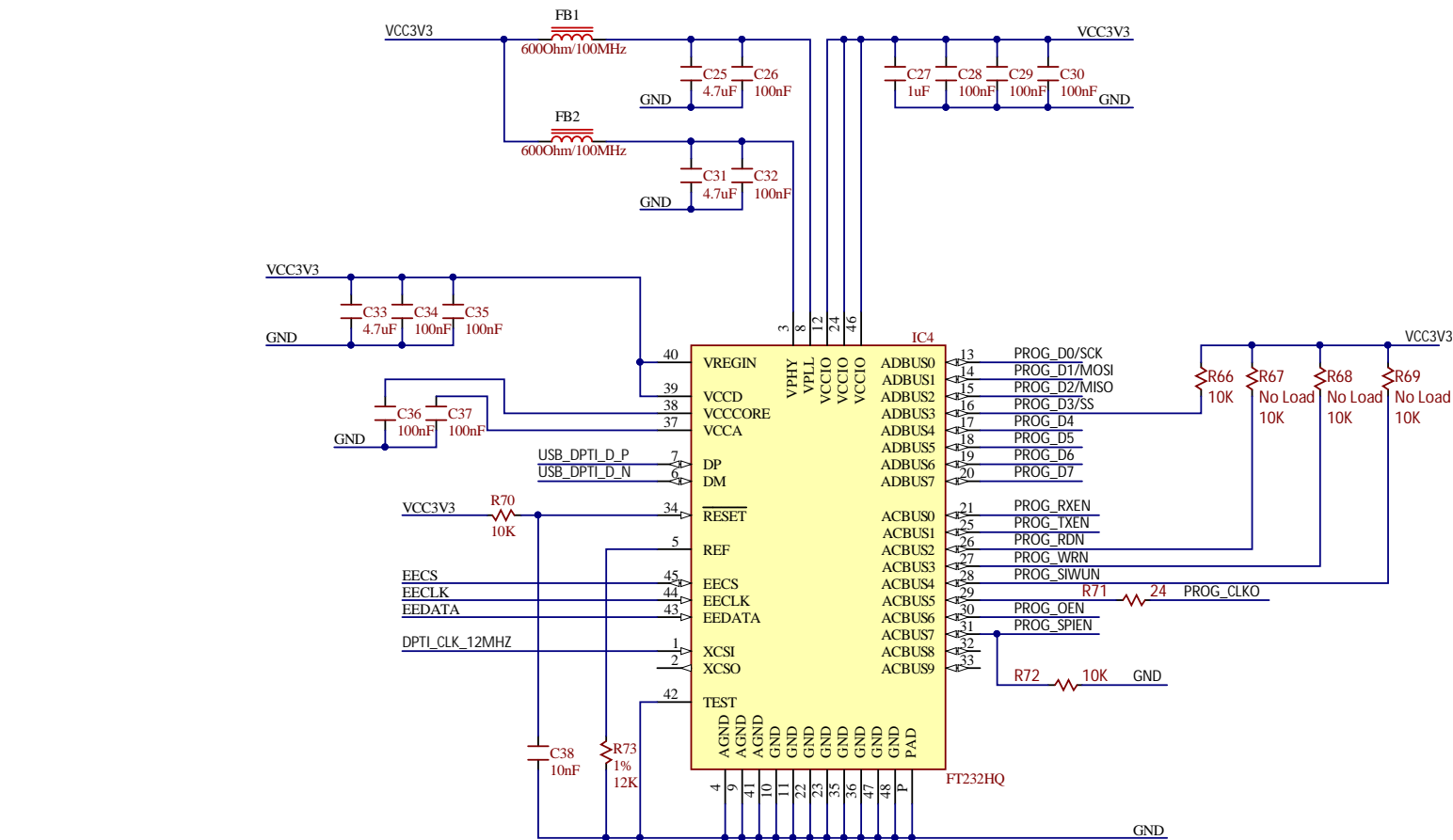
Note: CFG_SELx and NON_REMx are sampled on the rising edge of RESET_N

NOM_REM1	NOM_REMO	Port Configuration
0	0	All ports are removable
0	1	Port 1 is non-removable
1	0	Ports 1 and 2 are non-removable
1	1	When available, ports 1, 2, and 3 are non-removable



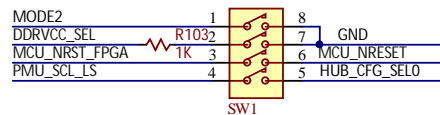
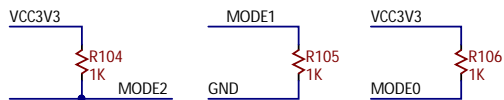
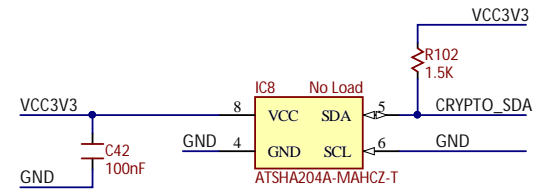
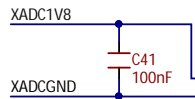
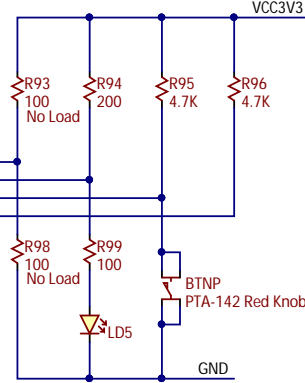
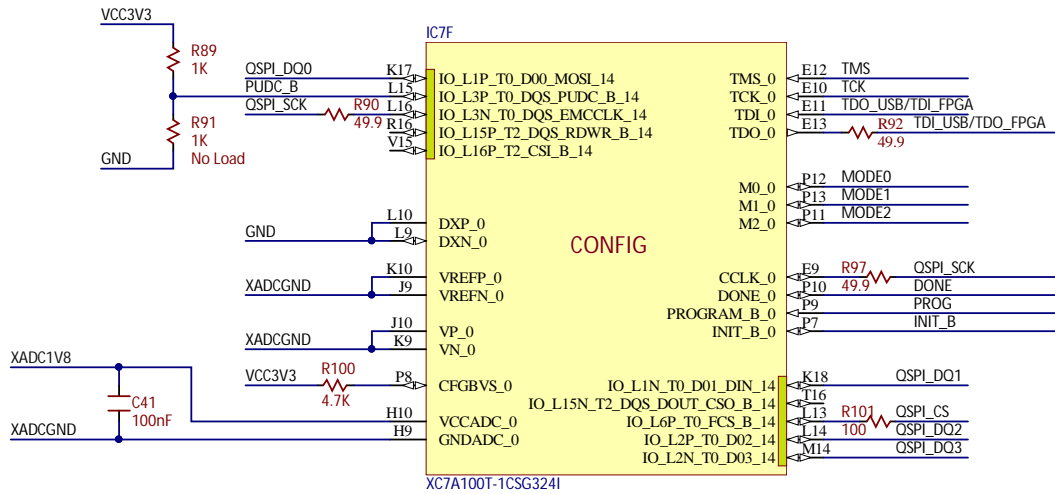
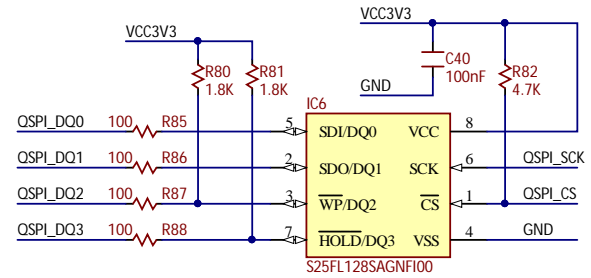
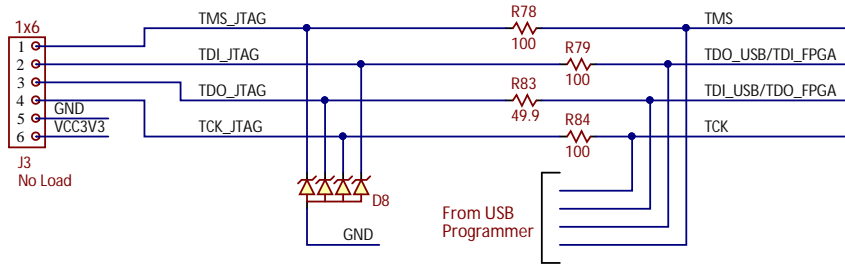
Note: Use of LOCAL_PWR requires the hub to be configured via SMBus or EEPROM.

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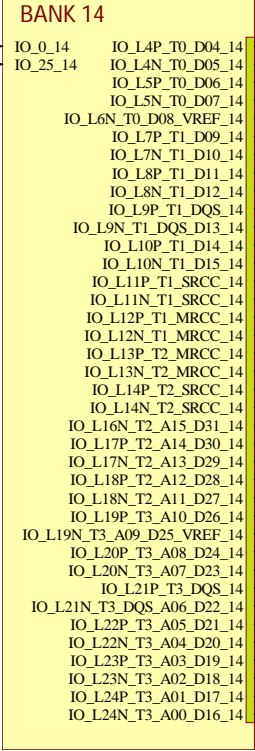




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CONFIG, SPI FLASH		
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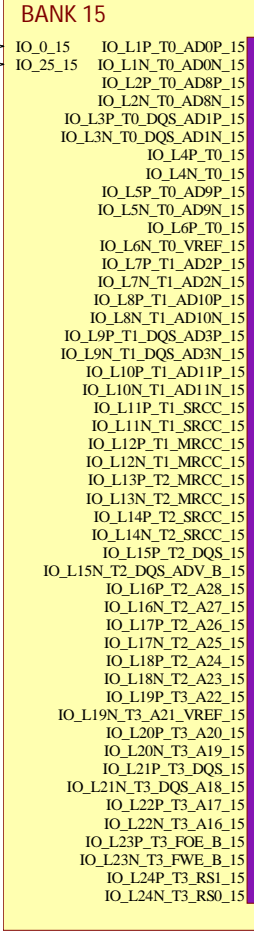


IC7A



XC7A100T-1CSG324I

IC7B

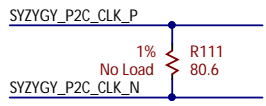


XC7A100T-1CSG324I

IC7C



XC7A100T-1CSG324I

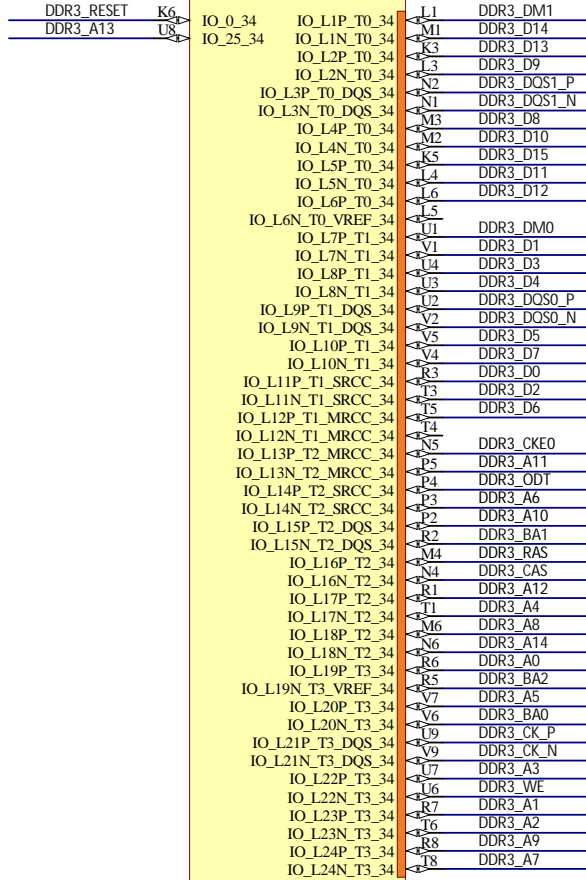


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IC7D

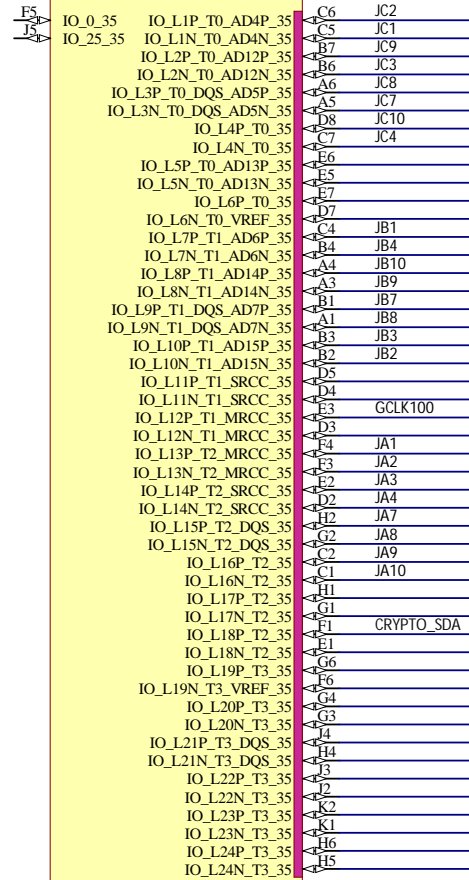
BANK 34



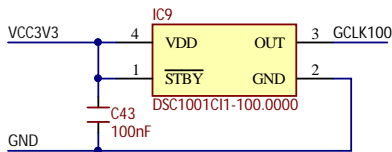
XC7A100T-1CSG324I

IC7E

BANK 35

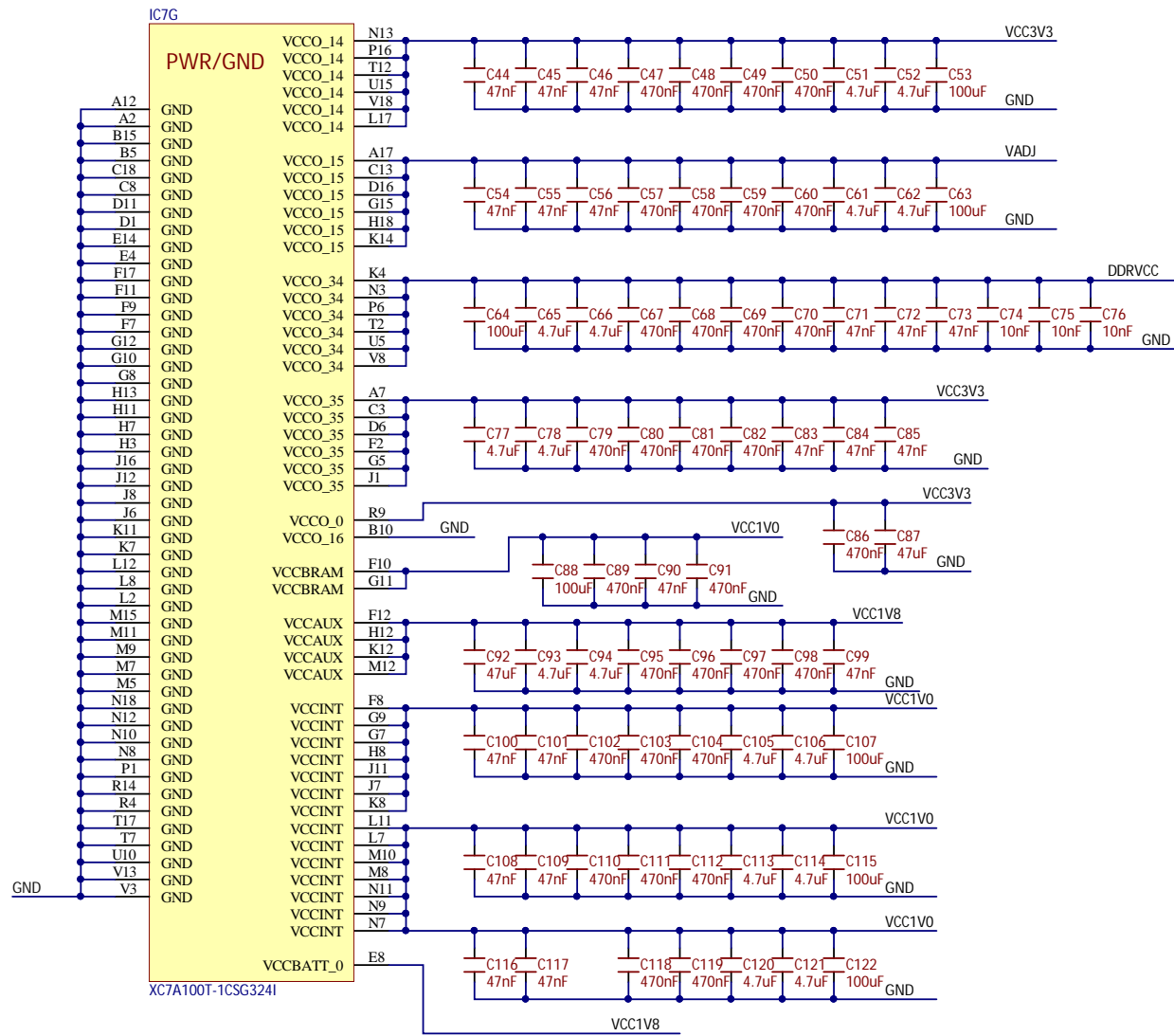


XC7A100T-1CSG324I



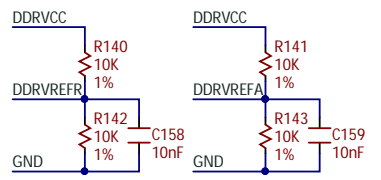
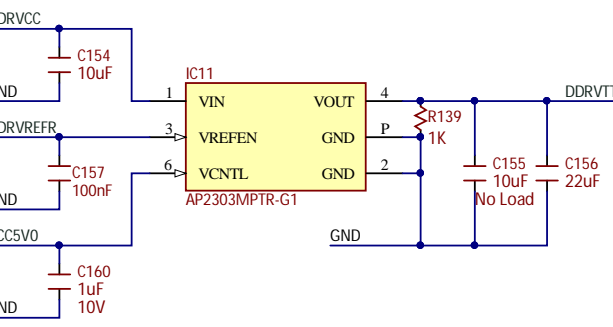
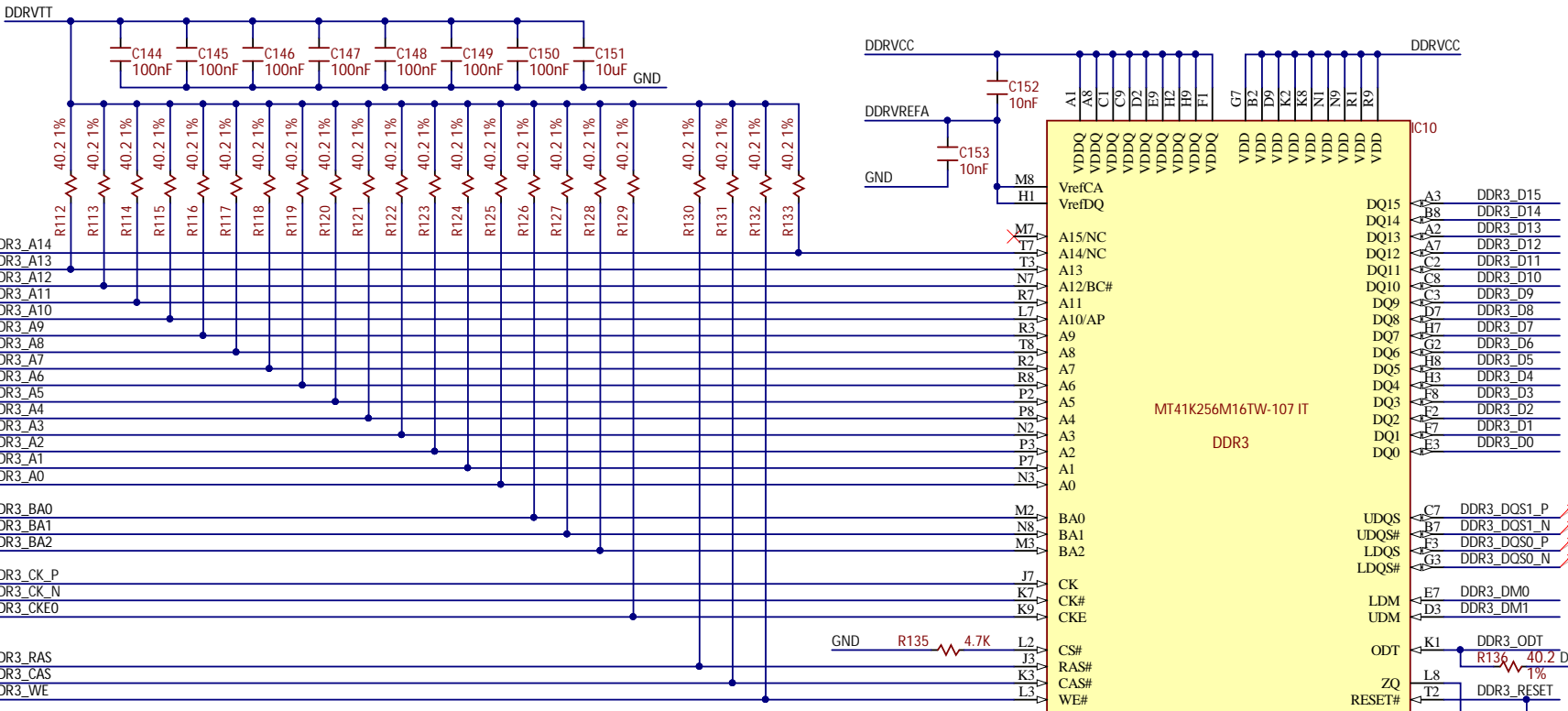
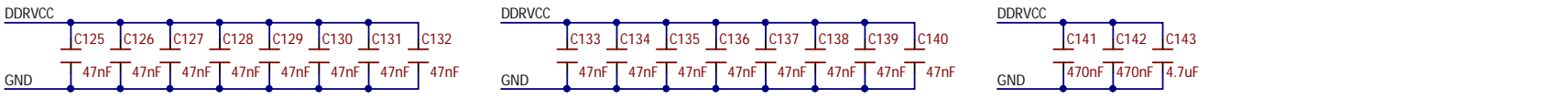
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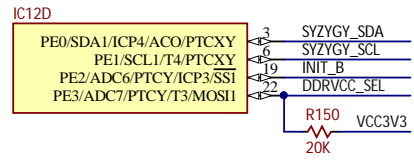
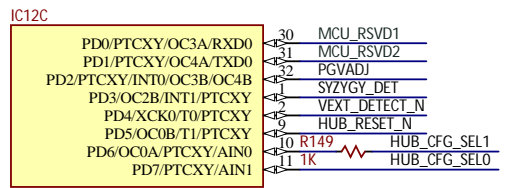
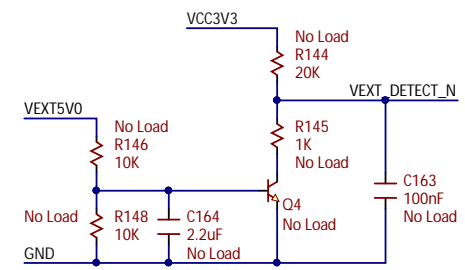
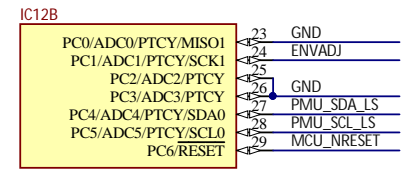
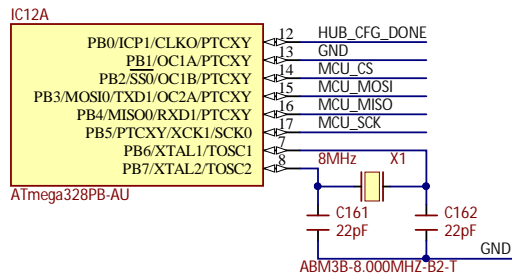


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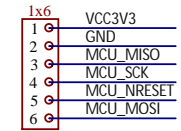
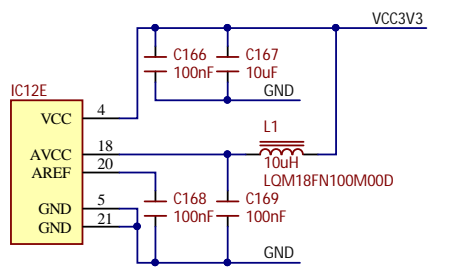
Title		Rev
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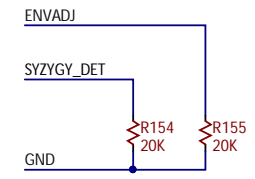
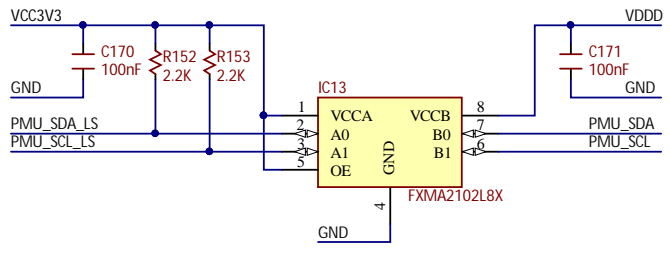
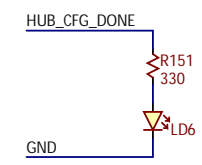
DDRVCC_SEL DDRVCC Voltage

0	1.35 Volts
1	1.50 Volts

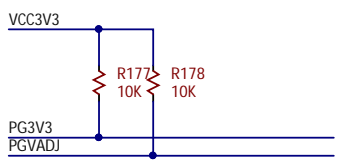
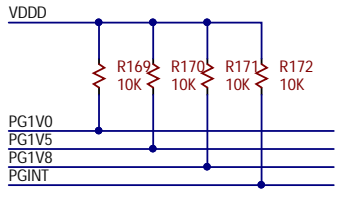
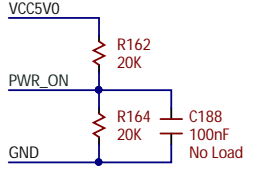
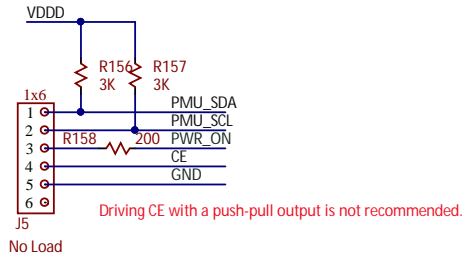
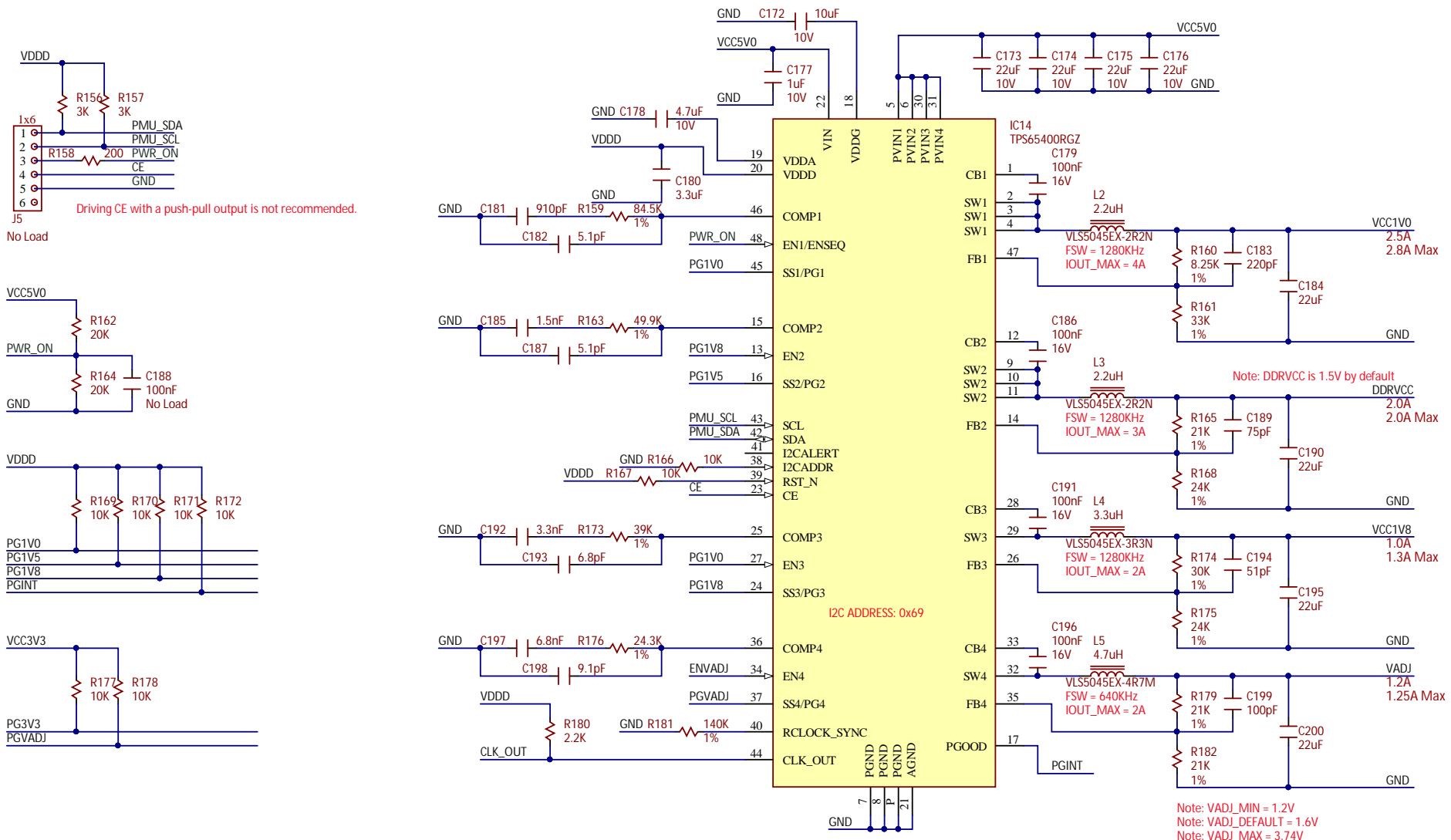
Note: DDRVCC_SEL is only sampled one time during each boot sequence.



Program/Debug using MPLAB SNAP Debugger
 Pin 2 of the SNAP connects to pin 1 on the board
 SNAP Pinout: <http://microchipdeveloper.com/pickit4:interface-pinouts>



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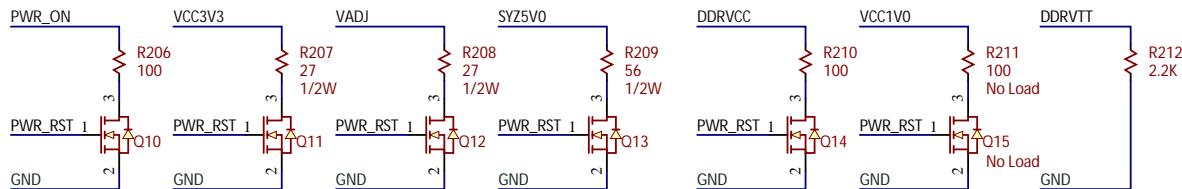
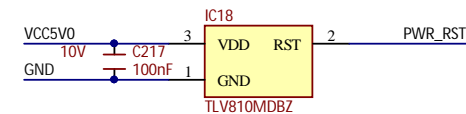
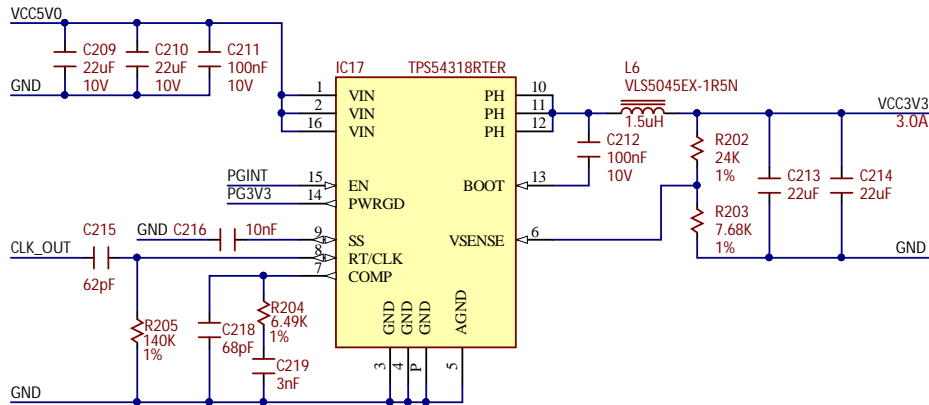
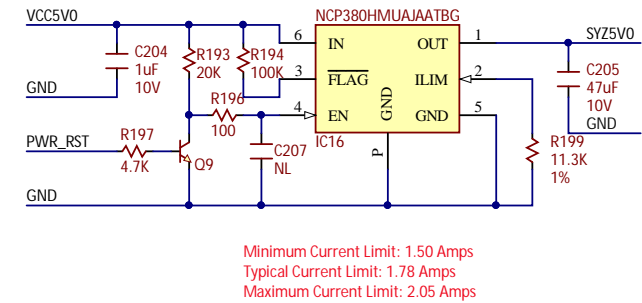
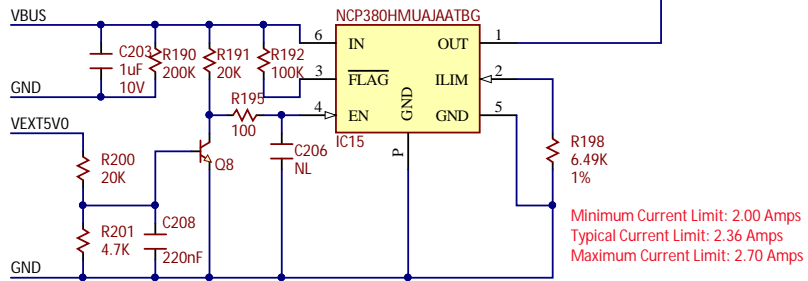
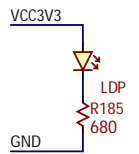
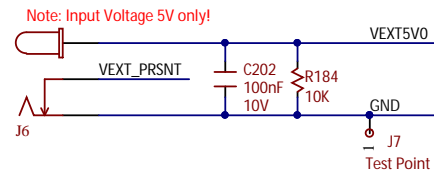
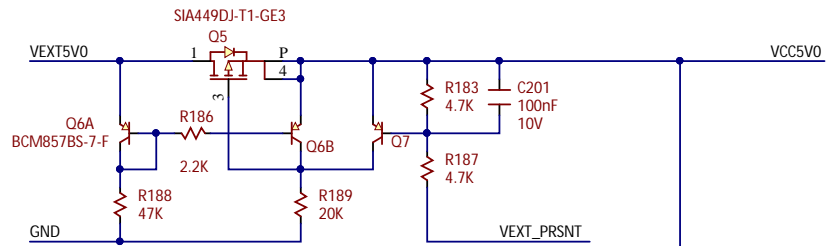


ISENSE_GAIN = 10A/V for all channels
 TON_RAMP_RATE = 0.25V/ms for all channels

Note: VADJ_MIN = 1.2V
 Note: VADJ_DEFAULT = 1.6V
 Note: VADJ_MAX = 3.74V

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