

# Table of Contents

<b>Table of Contents.....</b>	<b>iii</b>
<b>Preface.....</b>	<b>viii</b>
<b>Getting Started.....</b>	<b>9</b>
0.1 Breadboard .....	9
0.2 Power Supply.....	10
0.3 LEDs.....	10
0.4 Toggle Switches .....	11
0.5 Push Buttons.....	12
0.6 Debounced Push Buttons.....	12
0.7 Clock .....	13
0.8 Integrated Circuits .....	13
0.9 Circuit Construction .....	14
0.10 Materials and Parts .....	14
<b>Chapter 1: Introductory Concepts.....</b>	<b>16</b>
1.1 Introduction .....	16
1.2 Objectives .....	16
1.3 Discussion .....	16
1.3.1 Digital and Analog Circuits .....	16
1.3.2 Use of Binary Digital Ones and Zeros .....	18
1.3.3 Digital Circuits.....	19
1.4 Summary .....	21
1.5 Review Questions.....	21
<b>Chapter 2: Number Systems and Codes.....</b>	<b>22</b>
2.1 Introduction .....	22
2.2 Objectives .....	22
2.3 Discussion .....	22
2.3.1 The Binary Number System.....	23
2.3.2 Binary to Decimal Conversion.....	24
2.3.3 Decimal to Binary Conversion.....	24
2.3.4 The Hexadecimal Number System .....	25
2.3.5 The Octal Number System.....	26
2.3.6 Binary Coded Decimal System.....	26
2.3.7 ASCII Code .....	27
2.4 Summary .....	28
2.5 Review Questions.....	29
<b>Chapter 3: Logic Gates and Boolean Algebra.....</b>	<b>30</b>
3.1 Introduction .....	30
3.2 Objectives .....	30
3.3 Discussion .....	30
3.3.1 Boolean Variables.....	30
3.3.2 Truth Tables.....	30
3.3.3 The AND Operation.....	31
3.3.4 The OR Operation.....	32
3.3.5 The NOT Operation.....	32
3.3.6 Logic Equations .....	33
3.3.7 Logic Circuits .....	34
3.3.8 AND, OR and NOT Gates .....	34
3.3.9 NAND and NOR Gates.....	35

3.4	Summary .....	35
3.5	Review Questions .....	36
3.6	Lab Exercise 3.1: The NOT Gate (Inverter) .....	36
3.7	Lab Exercise 3.2: The And Gate.....	40
3.8	Lab Exercise 3.3: The OR Gate.....	41
3.9	Lab Exercise 3.4: The NAND Gate .....	41
3.10	Lab Exercise 3.5: The NOR Gate .....	42
3.11	Lab Exercise 3.6: Using the NAND Gate for Any Logic Function .....	43
3.12	Lab Exercise 3.7: Using the NOR Gate for Any Logic Function .....	44
<b>Chapter 4: Combinational Logic Circuits.....</b>		<b>46</b>
4.1	Introduction .....	46
4.2	Objectives .....	46
4.3	Sum-Of-Products Form .....	46
4.4	Designing Combination Circuits .....	47
4.5	Boolean Simplification .....	48
4.6	DeMorgan's Theorem.....	49
4.7	The Karnaugh Map.....	50
4.8	Don't Cares.....	55
4.9	Product-Of-Sums Form .....	56
4.10	The Exclusive OR And Exclusive NOR Circuits .....	59
4.11	Summary .....	59
4.12	Review Questions .....	60
4.13	Lab Exercise 4.1: Minterm and Maxterm Truth Tables.....	61
4.14	Lab Exercise 4.2: Simplifying Logic Circuits .....	63
4.15	Lab Exercise 4.3: Decoders .....	65
4.16	Lab Exercise 4.4: Multiplexers.....	66
4.17	Lab Exercise 4.5: The XOR Circuit .....	67
4.18	Lab Exercise 4.6: The XNOR Circuit.....	68
<b>Chapter 5: Latches and Flip-Flops.....</b>		<b>69</b>
5.1	Introduction .....	69
5.2	Objectives .....	69
5.3	Discussion .....	69
5.3.1	SR Latch .....	70
5.3.2	D Latch .....	71
5.3.3	SR Latch with Enable .....	72
5.3.4	D Latch with Enable .....	73
5.3.5	T Latch.....	73
5.3.6	JK Latch.....	74
5.3.7	Clock Signal.....	75
5.3.8	D Flip-Flop .....	76
5.3.9	JK Flip-Flop.....	77
5.3.10	Counting and Frequency Division .....	77
5.3.11	Monostable Multivibrators.....	78
5.4	Summary .....	78
5.5	Review Questions .....	78
5.6	Lab Exercise 5.1: SR Latches.....	79
5.7	Lab Exercise 5.2: The D Latch .....	81
5.8	Lab Exercise 5.3: The SR Latch with Enable.....	82
5.9	Lab Exercise 5.4: The D Latch with Enable .....	83
5.10	Lab Exercise 5.5: The D Flip-flop .....	84
5.11	Lab Exercise 5.6: The T Flip-flop .....	85
5.12	Lab Exercise 5.7: The J-K Flip-flop .....	86
5.13	Lab Exercise 5.8: The One-shot .....	88

<b>Chapter 6: Digital Arithmetic.....</b>	<b>90</b>
6.1 Introduction .....	90
6.2 Objectives .....	90
6.3 Discussion .....	90
6.3.1 Binary Addition .....	90
6.3.2 Signed Numbers.....	90
6.3.3 Binary Subtraction.....	91
6.3.4 Binary Multiplication.....	92
6.3.5 Binary Division.....	93
6.3.6 Hexadecimal Arithmetic .....	94
6.3.7 BCD Addition.....	94
6.3.8 The Half-adder.....	95
6.3.9 Full-adder.....	95
6.3.10 Parallel Binary Adder.....	96
6.3.11 BCD Adder .....	96
6.3.12 Binary Multipliers .....	97
6.4 Summary .....	97
6.5 Review Questions.....	97
6.6 Lab Exercise 6.1: Binary Adders.....	98
6.7 Lab Exercise 6.2: Parallel Binary Adder .....	99
6.8 Lab Exercise 6.3: The BCD Adder.....	101
6.9 Lab Exercise 6.4: The ALU.....	104
<b>Chapter 7: Counters and Registers.....</b>	<b>106</b>
7.1 Introduction .....	106
7.2 Objectives .....	106
7.3 Discussion .....	106
7.3.1 Ripple Counters .....	106
7.3.2 MOD Counters.....	107
7.3.3 Down Counters .....	108
7.3.4 Parallel Counters.....	108
7.3.5 Parallel UP/DOWN Counter.....	109
7.3.6 Presetable Counters.....	110
7.3.7 IC Binary UP/DOWN Counter .....	110
7.3.8 Counter Decoding.....	111
7.3.9 Shift Registers.....	111
7.3.10 Johnson Counter.....	112
7.3.11 Integrated Circuit Registers.....	113
7.4 Summary .....	115
7.5 Review Questions.....	115
7.6 Lab Exercise 7.1: UP/DOWN Counters .....	116
7.7 Lab Exercise 7.2: Synchronous Counters .....	117
7.8 Lab Exercise 7.3: IC Counters.....	118
7.9 Lab Exercise 7.4: Shift Registers.....	121
7.10 Lab Exercise 7.5: The 74LS165 .....	123
7.11 Lab Exercise 7.6: The 74LS164 .....	124
<b>Chapter 8: Integrated Circuit Logic Families.....</b>	<b>125</b>
8.1 Introduction .....	125
8.2 Objectives .....	125
8.3 Discussion .....	125
8.3.1 Terminology .....	125
8.3.2 TTL Logic Family .....	126
8.3.3 Standard TTL Logic Characteristics .....	128
8.3.4 TTL Loading Rules.....	129

8.3.5	Using Specification Sheets .....	129
8.3.6	Open Collector Outputs .....	131
8.3.7	Three-State Logic .....	133
8.3.8	Other TTL Families .....	134
8.3.9	The MOSFET .....	135
8.3.10	CMOS .....	136
8.3.11	Interfacing CMOS and TTL .....	137
8.3.12	ESD Control.....	138
8.4	Summary .....	138
8.5	Review Questions .....	139
8.6	Lab Exercise 8.1: TTL Loading Rules.....	139
8.7	Lab Exercise 8.2: Open-Collector Logic Gates .....	140
8.8	Lab Exercise 8.3: Three-State Logic .....	141
8.9	Lab Exercise 8.4: TTL and CMOS Interfacing .....	141
<b>Chapter 9: Medium Scale Integration .....</b>		<b>143</b>
9.1	Introduction .....	143
9.2	Objectives .....	143
9.3	Discussion .....	143
9.3.1	Decoders .....	143
9.3.2	BCD-to-Decimal Decoder .....	143
9.3.3	BCD-to-Seven Segment Display Decoders .....	144
9.3.4	Common Displays .....	145
9.3.5	Encoders .....	146
9.4	Multiplexers.....	147
9.4.1	Demultiplexers.....	150
9.4.2	3-State Registers .....	151
9.5	Summary .....	152
9.6	Review Questions .....	152
9.7	Lab Exercise 9.1: Decoders .....	152
9.8	Lab Exercise 9.2 .....	154
9.9	Lab Exercise 9.3: Encoders .....	155
9.10	Lab Exercise 9.4: Digital Multiplexers.....	156
9.11	Lab Exercise 9.5: Demultiplexers.....	157
<b>Chapter 10: Data Conversion and Acquisition .....</b>		<b>159</b>
10.1	Introduction .....	159
10.2	Objectives .....	159
10.3	Discussion .....	159
10.3.1	D/A Conversion .....	159
10.3.2	D/A Specifications .....	162
10.3.3	D/A Applications .....	163
10.3.4	A/D Conversion .....	163
10.3.5	Successive Approximation A/D .....	164
10.3.6	Data Acquisition .....	165
10.3.7	Sample and Hold Circuits .....	166
10.3.8	Multiplexing.....	166
10.4	Summary .....	168
10.5	Review Questions .....	168
10.6	Lab Exercise 10.1: D/A Converters.....	169
10.7	Lab Exercise 10.2 .....	170
10.8	Lab Exercise 10.3: The Analog Multiplexer .....	172
<b>Chapter 11: Potpourri.....</b>		<b>173</b>
11.1	Introduction .....	173
11.2	Objectives .....	173

11.3	Discussion .....	173
11.3.1	The 555 Timer.....	173
11.3.2	Opto-Isolators .....	175
11.3.3	DIP Relays .....	175
11.3.4	Programmable Logic Devices .....	175
11.4	Summary .....	178
11.5	Review Questions .....	178
11.6	Lab Exercise 11.1: The 555 Timer .....	178
11.7	Lab Exercise 11.2: DIP Relays .....	180
11.8	Lab Exercise 11.3: The Opto-Isolator .....	182
<b>Chapter 12: Microcomputer Concepts.....</b>		<b>183</b>
12.1	Introduction .....	183
12.1.1	Objectives .....	183
12.1.2	What Is A Microcomputer?.....	183
12.1.3	Organization of the Microcomputer .....	184
12.1.4	Interfacing.....	188
12.1.5	Parallel and Serial Data Transmission .....	188
12.1.6	Programming.....	190
12.1.7	Machine Language.....	192
12.1.8	Assembly Language .....	193
12.1.9	High Level Language.....	194
12.2	Summary .....	194
12.3	Review Questions .....	195
<b>Appendix A: IC Pin-outs.....</b>		<b>196</b>
<b>Appendix B: IC Chips Parts List.....</b>		<b>203</b>