Keysight W2630 Series DDR2 DRAM BGA Probes

Installation Guide

KEYSIGHT TECHNOLOGIES

Notices

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DDR2 DRAM BPA Probes – At a Glance

The DDR2 DRAM BGA probe enables logic analyzer state and timing measurements of all the DRAM buses, including the DQ, DQS, and clock signals of x8 and x16 DRAMs using the JEDEC standard common DDR2 DRAM footprint.

The probe interposes between the DRAM being probed and the PC board where the DRAM would normally be soldered. The probe is designed to be soldered to the PCB footprint for the DRAM. The DRAM being probed is then soldered to the top side of the probe.

Each DRAM signal in the common footprint (including those defined for x8 and x16 DRAMs) passes directly from the bottom side of the probe to the top side of the probe. Buried probe resistors placed at the DRAM balls connect the probed signals to the rigid flex to mate with an Keysight cable adapter (ZIF probe).

The W2630 Series probes are also compatible with the Keysight InfiniiMax oscilloscope probes. This allows oscilloscope probing of the DRAM signals with an Infiniium 54850, 80000, or 90000 Series oscilloscope, giving you a DDR2 testing solution covering the clock, electrical and timing parameters of the JEDEC specification. The W2631B and W2633B probes require the or W2639A adapter for oscilloscope probing.

The figures below show a probe and the adapter cable which connects the probe to a logic analyzer:

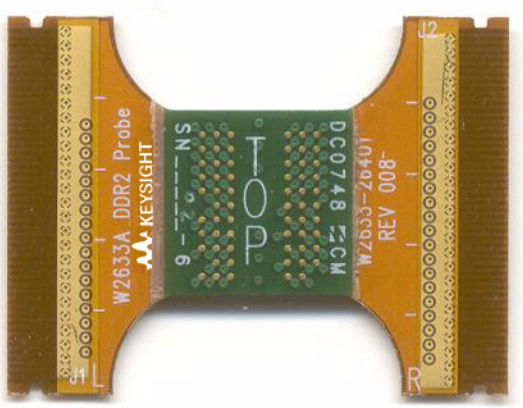

Figure 1 The W2633 DDR2 x8 BGA command and data probe can be used with a logic analyzer or an oscilloscope

Figure 2 The E5384A 46-channel single-ended x8/x16 DRAM BGA probe connects to a 90-pin logic analyzer cable

Technical Feature Summary

- Probing of DDR2 x8 and x16 DRAMs in BGA package using JEDEC standard common BGA footprint.
- Logic analyzer and oscilloscope connection to RAS, CAS, WE, DQ, DQS, DQS#, and CK/CK# signals.

  Logic analyzer connections are made using E5384A/E5826/7A single ended ZIF probe.

  Oscilloscope connections to the "A" Series probes are made using InfiniMax solder-in probe heads. Oscilloscope connections to the W2631B and W2633B probes are made using the W2639A adapter.
- Differential or single ended probing of DQS and CLK signals.
- Interposer design probes signals between DRAM BGA balls and DIMM.
- Use of separate E5384A, E5826A or E5827A single ended probes for connection to the logic analyzer optimizes use of analyzer channels by allowing assignment of analyzer channels to 8 or 16 bits on each DRAM.
- Tin plating of the DRAM footprint on the top side of the probe is compatible with both leaded and lead-free DRAM balls.

DDR3 Probes

Keysight offers equivalent probes for DDR3 memory:

- W3631A DDR3 x16 BGA address/control/data probe.

- W3633A DDR3 x4/x8 BGA address/control/data probe.
- E5845A adapter cable for W3631A probe.
- E5847A adapter cable for W3633A probe.
- W3635B DDR3 oscilloscope probe adapter.

The probes can be distinguished by the color of the printed circuit board: DDR2 probes are green and DDR3 probes are red.

In This Guide

This document provides installation information for the following Keysight products:

- W2631A/B DDR2 x16 command and data probe.
- W2632A DDR2 x16 BGA data probe.
- W2633A/B DDR2 x8 BGA command and data probe.
- W2634A DDR2 x8 BGA data probe.
- E5384A adapter cable adapter for 8x16 DRAM BGA.
- E5826A adapter cable for 2x16 DRAM BGA.
- E5827A adapter cable for 2x8 DRAM BGA.

Contents

1 Introduction

Equipment Required

You will need:

- Keysight 16900 Series logic analysis system.
- Keysight B4621A DDR2/3 decoder software.
- (optional) Keysight B4622A DDR2/3 protocol compliance and analysis tool.
- An appropriate number of Keysight 16950B, 16960A, or 16962A logic analyzer cards connected together as a module.
- One or more W2630 Series BGA probes.
- One or more E5380 Series adapter cables.
- (optional) Oscilloscope with solder-in or ZIF probes.
- (optional) One or more W2639A adapters for oscilloscope probing when using the W2631B or W2633B probes.

The following table shows how many DRAM BGA probes and cable adapters are required to provide connections to all channels of your logic analyzer module.

Table 1 Number of DRAM BGA probes and cable adapters required

DRAM	Data Width	Probes	Cables	Number of LA modules
x8	x8	W2633A/B	E5384A	16950B
				16950B
x8	x16	W2633A/B	E5384A	16950B
		W2634A	E5827A	16950B
x8	x32	W2633A/B	E5384A	16950B
				16950B
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	

DRAM	Data Width	Probes	Cables	Number of LA modules
x8	x64	W2633A/B	E5384A	16950B
				16950B
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
x8	x72	W2633A/B	E5384A	16950B
				16950B
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		

DRAM	Data Width	Probes	Cables	Number of LA modules
x8	x144	W2633A/B	E5384A	16950B
		W2634A	E5827A	16950B
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
x16	x16	W2631A/B	E5384A	16950B
				16950B
x16	x32	W2631A/B	E5384A	16950B
		W2632A	E5826A	16950B
x16	x64	W2631A/B	E5384A	16950B
		W2632A	E5826A	16950B
		W2632A	E5826A	
		W2632A	E5826A	16950B

DRAM	Data Width	Probes	Cables	Number of LA modules
x16	x128	W2631A/B	E5384A	16950B
		W2632A	E5826A	16950B
		W2632A	E5826A	16950B
		W2632A	E5826A	
		W2632A	E5826A	16950B
		W2632A	E5826A	
		W2632A	E5826A	16950B
		W2632A	E5826A	

Mechanical Considerations

Keep-Out Volume

The following figures show the KOV of the Keysight E5384A, E5826, E5827A logic analyzer cable adapters when connected to the W2630 Series DDR2 DRAM BGA probe.

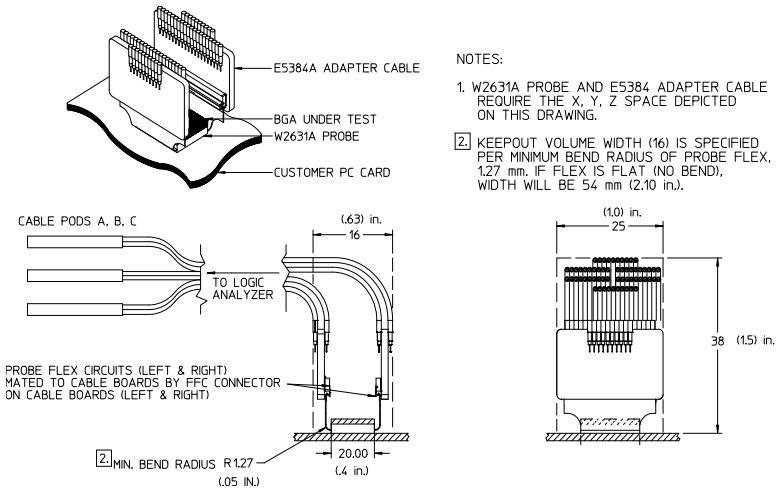

Figure 3 KOV of W2631A/B with E5384A

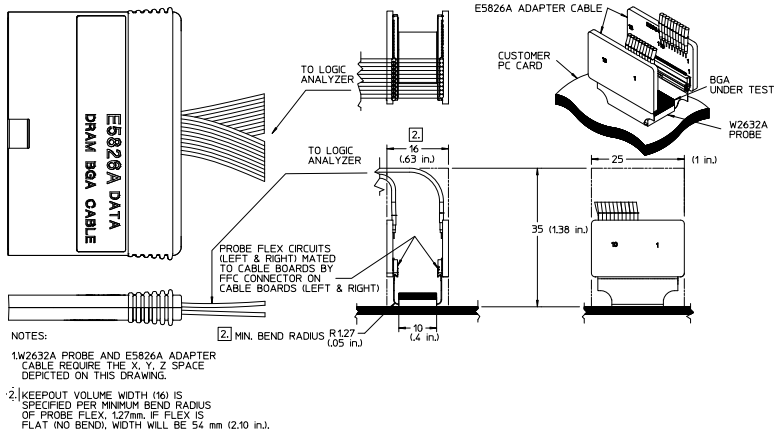

Figure 4 KOV of W2632A with E5826A

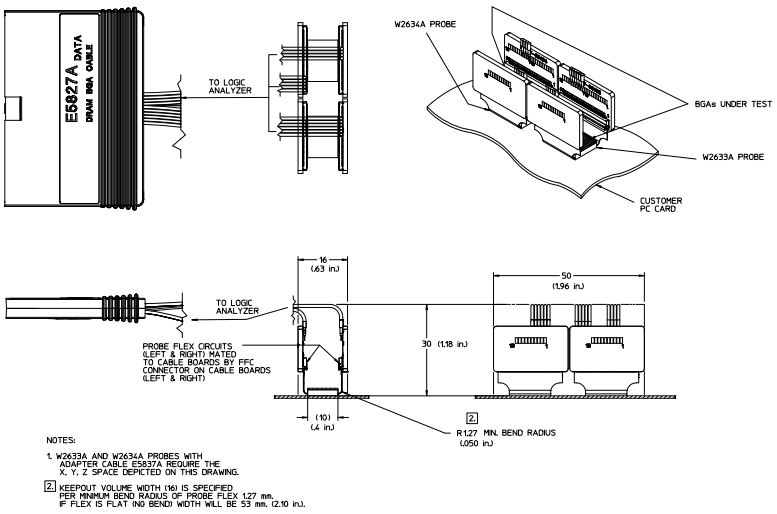

Figure 5 KOV of W2633A/B, W2634A, and E5827A

Probe Dimensions

The following figures show the dimensions of the Keysight W2631A, W2632A, W2633A and W2634A DRAM BGA probes.

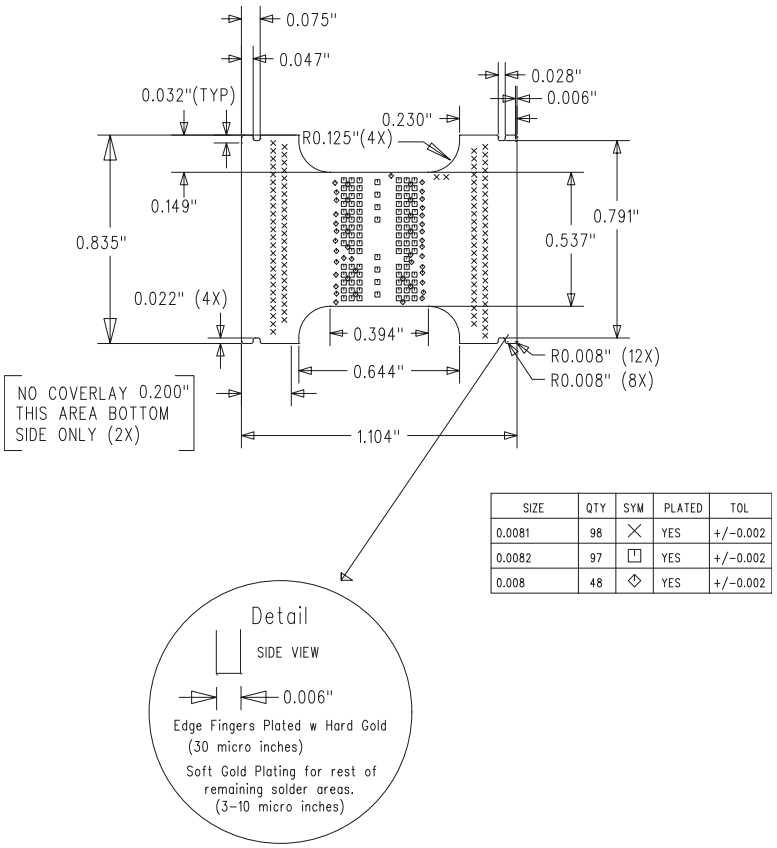

Figure 6 Dimensions of W2631A and W2632A probes

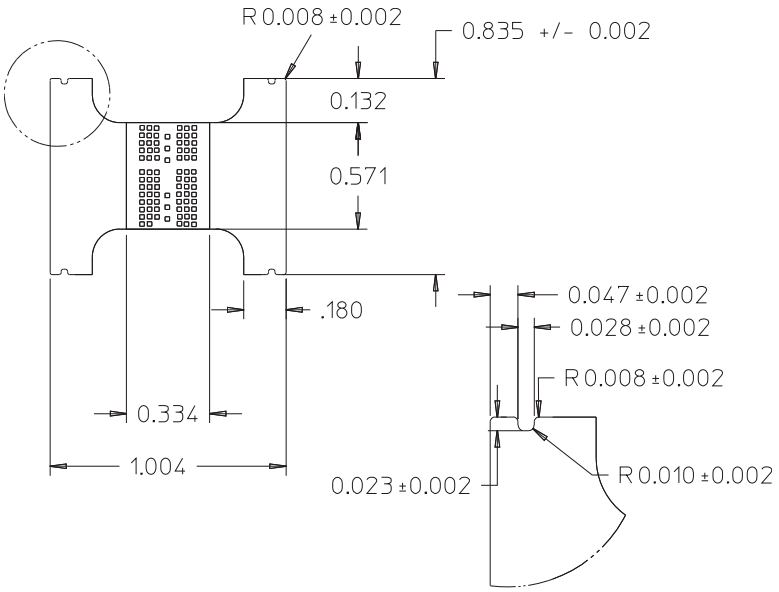

Figure 7 Dimensions of W2631B probe

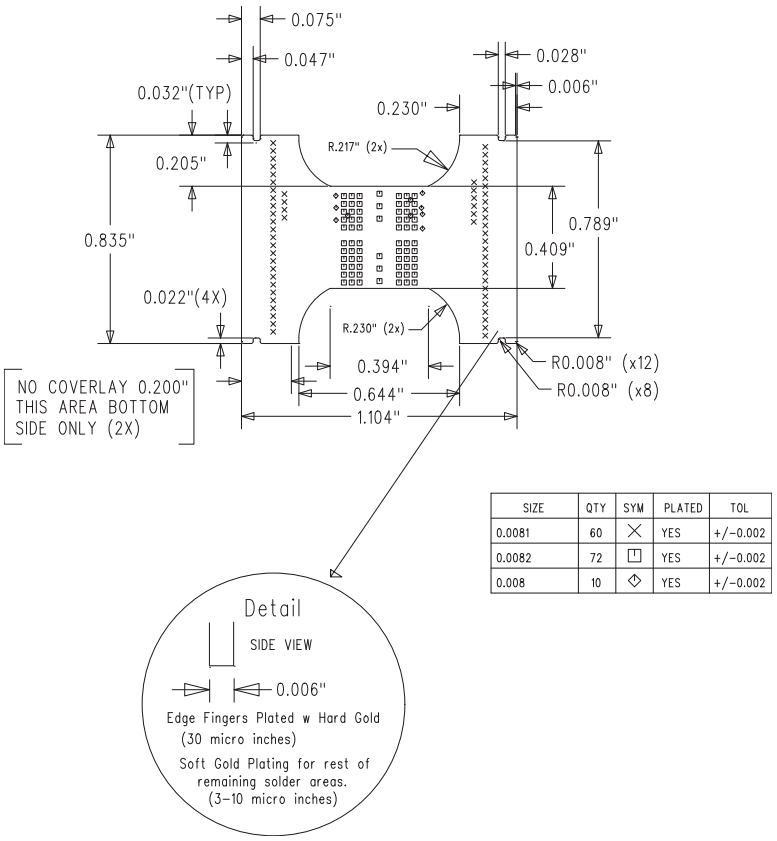

Figure 8 Dimensions of W2633A and W2634A probes

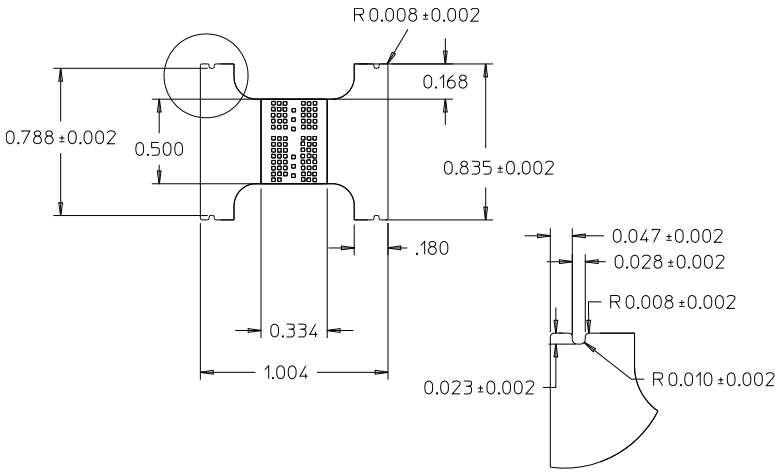

Figure 9 Dimensions of W2633B probe

Board and Wings Thickness

- Board thickness - 0.072 inches (+/-10% for maximum variation)
- Thickness above the wing (Layer1-4) - 0.0365
- Thickness below the wing (Layer 7-9) - 0.0194

2 Installing the Probe

Soldering the BGA Probe

Order of Installation

The W2631/2/3/4 BGA probes need to be attached to the DRAM PCB footprint on the design to be probed, and the desired DRAM is soldered to the top side of the probe. This attachment may occur in any order:

- first solder the probe to the DUT, and then solder the DRAM to the probe, or
- first solder the DRAM to the probe, and then solder the DRAM+probe assembly to the DUT.

Solder Temperature

The probe is design to tolerate lead-free soldering temperature profiles. However, it is always recommended to apply the minimum temperature required and the minimum number of heating/cooling cycles to reduce risk of any damage to the probe.

Recommended soldering guidelines:

1 The maximum temperature that the BGA probe can withstand is 260 °C.

2 Bake out the boards and components to eliminate moisture entrapment. Normally bake for 24 hours at 125 °C or to the component or board specification.

Solder Composition

The probe is supplied without solder balls. Depending on the exact attachment order, either leaded or lead-free solder may be preferred to attach the probe to the DUT. The design of the probe supports either choice.

Soldering Recommendations

The flexible “wings” on the probe may need to be bent upwards before soldering to avoid mechanical contact with components adjacent to the probe on the DUT. This will also ensure reliable connection when connect to the logic analyzer cable adapters.

If the in-house expertise to attach the BGA probe and DRAM cannot be found, there are contract manufacturers with this expertise who may be willing to perform the attachment for a fee. More information on BGA soldering and rework techniques that may be useful in attaching the probe may be found at: "http://www.circuitrework.com/guides/9-0.shtml"

Connecting the BGA Probe to a Logic Analyzer

The E5384A and E5826/7A adapter cables are used with the W2630 Series BGA probe to connect the probe to the logic analyzer.

1 Check that you have the correct adapter cable for the BGA probe you are using.
2 Connect the adapter cable to the BGA probe.
3 Connect the adapter cable to the 90-pin logic analyzer pod cable.

NOTE Please ensure that the wings on the BGA probe are properly latched to the ZIF connectors on the E5384A and E5826/7A adapter cables. The ZIF connectors can withstand up to 50 cycles of insertions. Please handle the probe with care.

Logic Analyzer Channel Mapping

The following tables show where each signal appears on the logic analyzer. The signals are automatically configured when you load one of the configuration files supplied with the Keysight B4621A decoder.

Table 2 Logic Analyzer Channel Mapping for the E5384A Probe Cable

Data Pod / Pod A		Control Pod / Pod B		Address Pod / Pod C	
LA Channel	Signal Name	LA Channel	Signal Name	LA Channel	Signal Name
0	DQ0	0	CS#	0	SPARE1
1	DQ1	1	CAS#	1	SPARE2
2	DQ2	2	RAS#	2	RFU#2
3	DQ3	3	ODT	3	A12
4	DQ4	4	BA2	4	A11
5	DQ5	5	BA0	5	A10
6	DQ6	6	BA1	6	A9
7	DQ7	7	CKE	7	A8
8	DQ8	8	WE#	8	A7
9	DQ9	9	VREF	9	A6
10	DQ10	10	LDM	10	A5
11	DQ11	11	UDM	11	A4
12	DQ12	12	-	12	A3
13	DQ13	13	-	13	A2
14	DQ14	14	-	14	A1
15	DQ15	15	-	15	A0
Clock_P	LDQS	Clock_P	CK	Clock_P	-
Clock_N	LDQS#	Clock_N	CK#	Clock_N	-

Table 3 Logic Analyzer Channel Mapping for the E5826A Probe Cable

Data Pod	
LA Channel	**Signal Name**
0	DQ0
1	DQ1
2	DQ2
3	DQ3
4	DQ4
5	DQ5
6	DQ6
7	DQ7
8	DQ8
9	DQ9
10	DQ10
11	DQ11
12	DQ12
13	DQ13
14	DQ14
15	DQ15
Clock_P	LDQS
Clock_N	LDQS#

Table 4 Logic Analyzer Channel Mapping for the E5827A Probe Cable

Data Pod	
LA Channel	**Signal Name**
0	DQ0 (Probe #1)
1	DQ1 (Probe #1)
2	DQ2 (Probe #1)
3	DQ3 (Probe #1)
4	DQ4 (Probe #1)
5	DQ5 (Probe #1)
6	DQ6 (Probe #1)
7	DQ7 (Probe #1)
8	DQ8 (Probe #2)
9	DQ9 (Probe #2)
10	DQ10 (Probe #2)
11	DQ11 (Probe #2)
12	DQ12 (Probe #2)
13	DQ13 (Probe #2)
14	DQ14 (Probe #2)
15	DQ15 (Probe #2)
Clock_P	LDQS (Probe #1)
Clock_N	LDQS# (Probe #1)

Connecting the BGA Probe to an Oscilloscope

How to Connect the Oscilloscope to "A" Series Probes

The BGA probes incorporate a set of pads to which oscilloscope probes may be soldered. Several options are available for connecting an oscilloscope: solder-in probes or ZIF probes.

Solder-in probe Use a high-bandwidth solder-in probe to connect the oscilloscope to the pads on the BGA probe. The following probes are recommended:

- Keysight N5381A InfiniiMax II 12 GHz differential solder-in probe head. (Recommended for use with 1130/31/32/34A InfiniiMax probe amplifier.)
- Keysight E2677A InfiniiMax 12 GHz differential solder-in probe head. (Recommended for use with InfiniiMax II 1168A/69A probe amplifier.)

ZIF probe An alternative is to solder a ZIF probe head onto the pads on the BGA probe and probe with a ZIF probe tip. The following probe is recommended:

- Keysight N5425A 12 GHz InfiniiMax differential ZIF probe head with the Keysight N5426A 12 GHz InfiniiMax ZIF Tip.

Where to Connect the Oscilloscope: W2631A

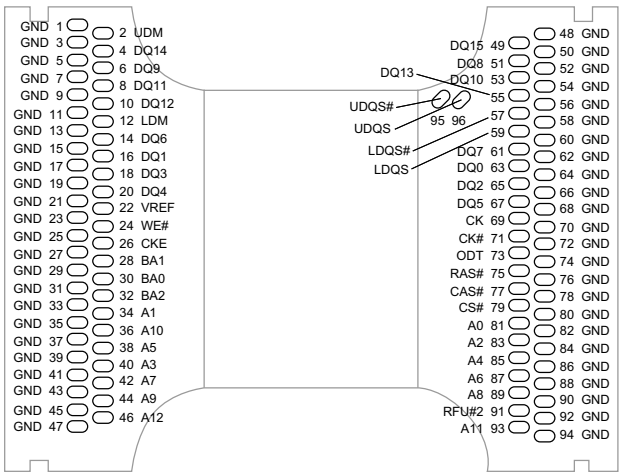

Figure 10 W2631A pad numbering as seen through the board from the top side of the probe

Where to Connect the Oscilloscope: W2631B, W2633B

The primary method of connecting the oscilloscope to the W2631B and W2633B probes is using the W2639A adapter. See:

- "Using the W2639A Adapter" on page 26
- "Reworking the W2639A Adapter for W2631A/B and W2633A/B Probes" on page 27

There are, however, a few test points on the BGA probes for signals that are not available on the W2639A adapter. The signal names are silkscreened by the test points.

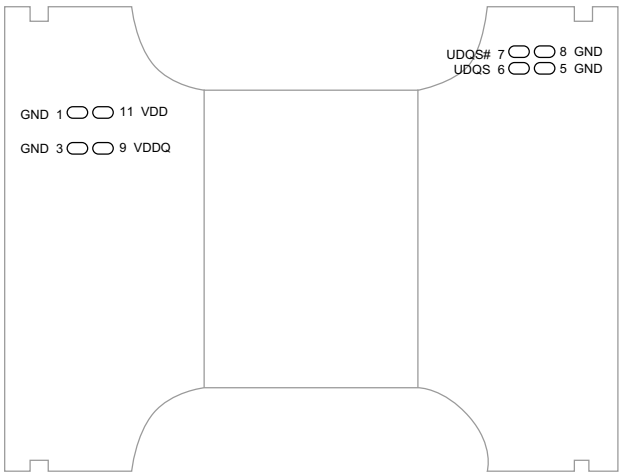

Figure 11 W2631B and W2633B pad numbering as seen through the board from the top side of the probe

Where to Connect the Oscilloscope: W2632A

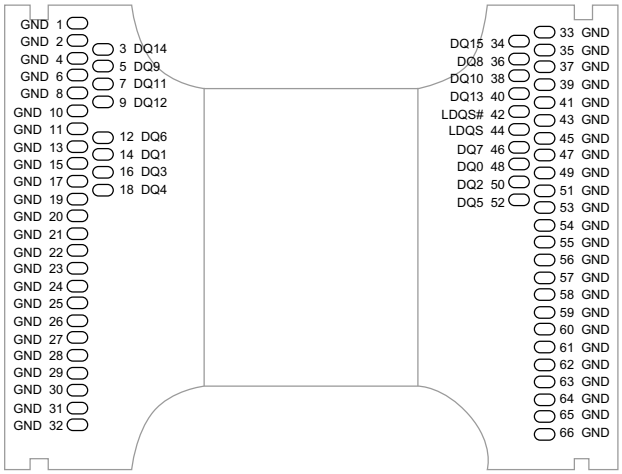

Figure 12 W2632A pad numbering as seen through the board from the top side of the probe

Where to Connect the Oscilloscope: W2633A

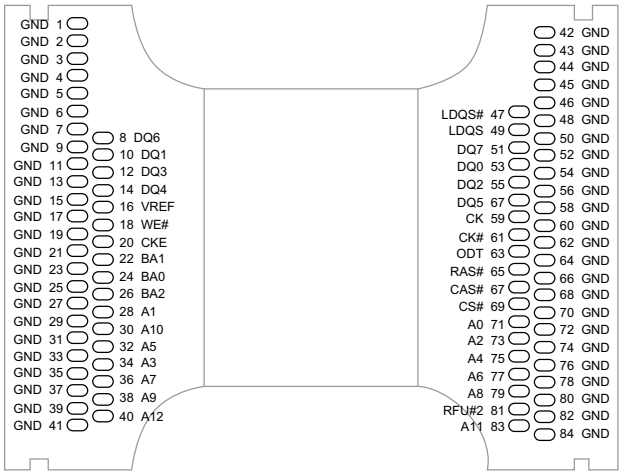

Figure 13 W2633A pad numbering as seen through the board from the top side of the probe

Where to Connect the Oscilloscope: W2634A

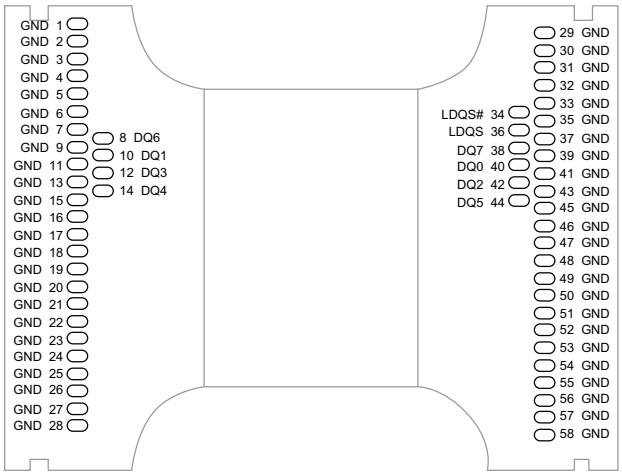

Figure 14 W2634A pad numbering as seen through the board from the top side of the probe

Using the W2639A Adapter

The W2631B and W2633B DDR2 BGA probes may be used with Keysight E2678A socketed probe head with damping header to provide connection to the oscilloscope.

A few additional signals may be probed by soldering the oscilloscope probe directly to a test point on the BGA probe.

The E2678A socketed probe head makes a 2 GHz bandwidth connection with the test point on the adapter or BGA probe.

Signals probed by the W2639A adapter

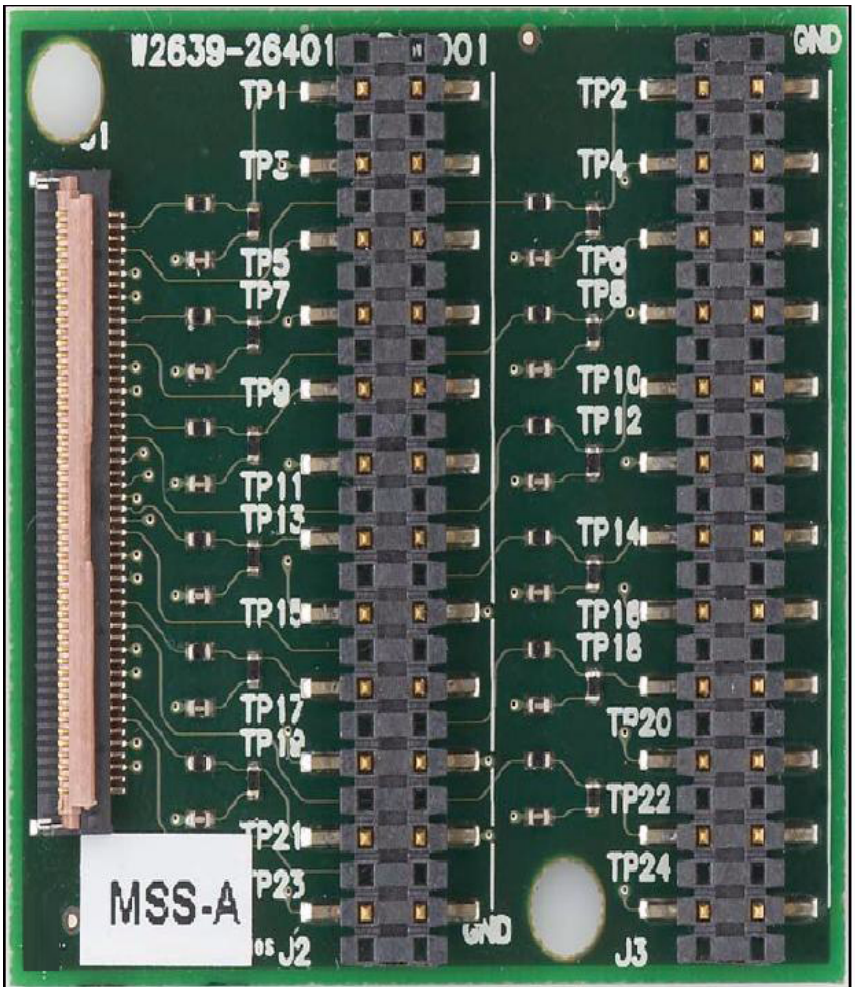

Figure 15 W2639A

Reworking the W2639A Adapter for W2631A/B and W2633A/B Probes

The W2639A adapter is designed to provide high bandwidth performance to the oscilloscope with proper termination. However, for use with the W2631A and W2633A DDR2 BGA probes, the VREF point should not be terminated. These rework instructions provide a workaround to correct the termination point of VREF at the W2639A oscilloscope probe board adapter.

The figure below shows the overall features and connection points for the probe:

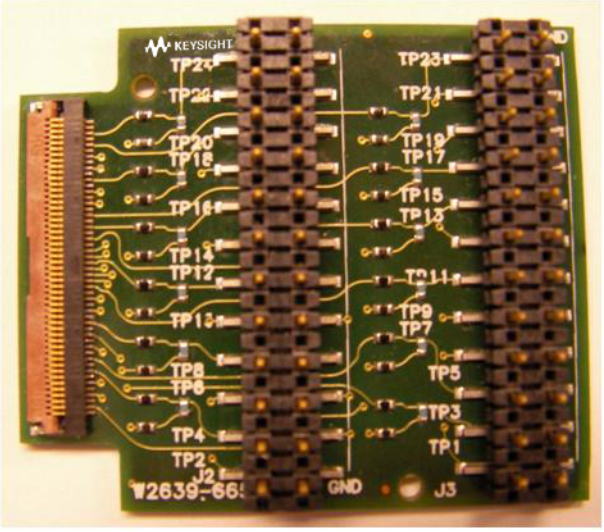

Figure 16 W2639A oscilloscope probe adapter board

Equipment required for rework:

- W2639A oscilloscope probe board adapter (1 of 2).
- Soldering iron.

To remove the VREF termination on the W2639A DDR2 oscilloscope probe board adapter for use with the W2631A DDR2 x16 BGA probe:

1 The VREF signal is connected to the W2639A oscilloscope probe board adapter via the left flex wing of the W2631A DDR2 BGA probe on TP11 as shown in Table 1.

2 Remove the 37.4 ohm resistor located near TP11 with a soldering iron as shown in the following figure to disconnect the signal from GND. This will open the path to VREF.

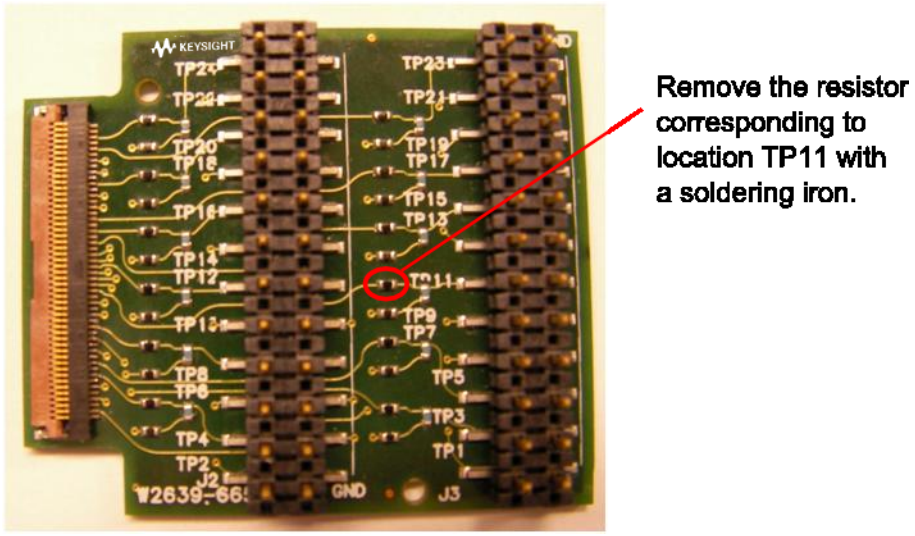

Figure 17 Location of the 37.4 ohm resistor for TP11 on the W2639A oscilloscope probe board adapter

3 Label the reworked W2639A oscilloscope probe adapter board "LEFT". The reworked W2639A must only connect to the left flex wing of the W2631A DDR2 BGA probe.

4 The rework instruction may be repeated for the following BGA probes with reference to the pinout tables shown in the user manual:
"http://cp.literature.keysight.com/litweb/pdf/W2638-97000.pdf"

- W2631A x16 DDR2 BGA probe.
- W2633A x8 DDR2 BGA probe.

Note: Please contact Keysight to confirm the exact location of the resistor.

Table 5 W2639A LPDDR BGA Probe Adapter Board Pin-Out for DDR2 Interposer Configuration (W2631A/B)

Left Flex Wing						Right Flex Wing					
Signal Name	Signal Name	Test Point	Signal Name	Signal Name	Test Point	Test Point	Signal Name	Signal Name	Test Point	Signal Name	Signal Name
GND	UDM	TP1	GND	DQ14	TP2	TP24	DQ15	GND	TP23	DQ8	GND
GND	DQ9	TP3	GND	DQ11	TP4	TP22	DQ10	GND	TP21	DQ13	GND
GND	DQ12	TP5	GND	DQ6	TP6	TP20	LDQS#	GND	TP19	DQ7	GND
GND	LDM	TP7	GND	DQ1	TP8	TP18	LDQS	GND	TP17	DQ0	GND
GND	DQ3	TP9	GND	DQ4	TP10	TP16	DQ2	GND	TP15	DQ5	GND
GND	VREF	TP11	GND	CKE	TP12	TP14	CK	GND	TP13	ODT	GND
GND	WE#	TP13	GND	BA1	TP14	TP12	CK#	GND	TP11	RAS#	GND
GND	BA0	TP15	GND	BA2	TP16	TP10	CAS#	GND	TP9	CS#	GND
GND	A1	TP17	GND	A5	TP18	TP8	A0	GND	TP7	A4	GND
GND	A10	TP19	GND	A3	TP20	TP6	A2	GND	TP5	A6	GND
GND	A7	TP21	GND	A9	TP22	TP4	A8	GND	TP3	RFU#2	GND
GND	A12	TP23	GND	NC	TP24	TP2	A11	GND	TP1	NC	GND

Table 6 W2639A LPDDR BGA Probe Adapter Board Pin-Out for DDR2 Interposer Configuration (W2633A/B)

Left Flex Wing						Right Flex Wing					
Signal Name	Signal Name	Test Point	Signal Name	Signal Name	Test Point	Test Point	Signal Name	Signal Name	Test Point	Signal Name	Signal Name
GND	NC	TP1	GND	NC	TP2	TP24	NC	GND	TP23	NC	GND
GND	NC	TP3	GND	NC	TP4	TP22	NC	GND	TP21	NC	GND
GND	NC	TP5	GND	DQ6	TP6	TP20	LDQS#	GND	TP19	DQ7	GND
GND	NC	TP7	GND	DQ1	TP8	TP18	LDQS	GND	TP17	DQ0	GND
GND	DQ3	TP9	GND	DQ4	TP10	TP16	DQ2	GND	TP15	DQ5	GND
GND	VREF	TP11	GND	CKE	TP12	TP14	CK	GND	TP13	ODT_0	GND
GND	WE#	TP13	GND	BA1	TP14	TP12	CK#	GND	TP11	RAS#	GND
GND	BA0	TP15	GND	BA2	TP16	TP10	CAS#	GND	TP9	CS#	GND
GND	A1	TP17	GND	A5	TP18	TP8	A0	GND	TP7	A4	GND
GND	A10	TP19	GND	A3	TP20	TP6	A2	GND	TP5	A6	GND
GND	A7	TP21	GND	A9	TP22	TP4	A8	GND	TP3	RFU#2	GND
GND	A12	TP23	GND	NC	TP24	TP2	A11	GND	TP1	NC	GND

3 Setting Up the Logic Analysis System

Installing Logic Analysis Software

1. The software is licensed. If the software is not already installed, make sure you have the Entitlement Certificate. If the software came preinstalled on the logic analysis system, no further action is required to license it, but you should still update to the latest version of the software.
2. Get the latest version of the logic analyzer application, the B4621A decoder, and the B4622A compliance software from the web at: "http://www.keysight.com/find/la-sw-download"
3. After you have downloaded the software, double-click on the setup file then follow the instructions which are displayed.
4. Follow the instructions on the Entitlement Certificate to redeem your license and enable the application.

The software is documented in the online help.

Keysight B4621A DDR Memory Bus Decoder

The Keysight B4621A DDR memory bus decoder allows you to view transactions, commands, and data from a DDR2 or DDR3 memory bus.

The DDR data bus is displayed as raw hexadecimal data. The decoder does not inverse assemble the data payload.

Sample Number	Physical Address	DDR Bus Decode	Cycle Type
17461			Idle
17462		Deselect	Idle
17463			Idle
17464		Deselect	Idle
17465			Idle
17466	00 2000	Write CS-0 BA-0	Command
17466.1		Row Address = 0x020	*
17466.2		Col Address = 0x00	*
17466.3		Burst Type = Sequential (0, 1, 2, 3, 4, 5.	*
17466.4	00 2000	mem write 0x00	*
17466.5	00 2001	mem write 0x00	*
17466.6	00 2002	mem write 0x00	*
17466.7	00 2003	mem write 0x00	*
17466.8	00 2004	mem write 0x00	*
17466.9	00 2005	mem write 0x00	*
17466.10	00 2006	mem write 0xff	*
17466.11	00 2007	mem write 0x00	*
17467			Idle
17468		Deselect	Idle
17469			Idle
17470		Deselect	Idle
17471			Idle
17472		Deselect	Idle
17473			Idle
17474		Deselect	Idle
17475			Idle
17476		Deselect	Data Write
17477			Data Write
17478		Deselect	Data Write
17479			Data Write
17480		Deselect	Data Write
17481			Data Write
17482		Deselect	Data Write

Figure 18 A screen from the DDR decoder showing decoded memory writes

Keysight B4622A DDR2/3 Protocol Compliance and Analysis Tool

This package consists of three tools:

- A trigger tool, which automatically sets up a trigger on the address you specify.
- A validation tool, which evaluates captured DDR2/DDR3 data against a set of user- defined limits to help you validate that a memory system is operating properly. The automated test application guides you through the process of selecting and configuring tests, running tests, and evaluating the test results.
- A performance tool, which graphically profiles the distribution of memory accesses.

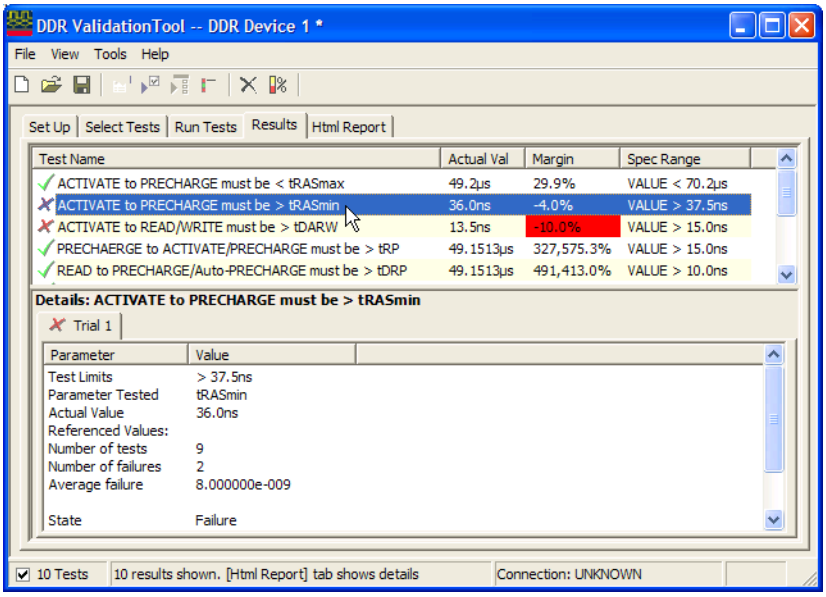

Figure 19 A screen from the DDR validation tool showing results from a bus where the Activate-to-Precharge time is less than tRASmin as specified in the JEDEC standard.

Configuration Files

The mapping of specific signals to logic analyzer channels depends on:

- Which DRAMs on a DIMM are probed.
- Which probe you are using.
- How the single ended logic analyzer cable adapters are arranged when connecting to the DDR2 DRAM BGA probe.

Because of these dependencies, there is no single logic analyzer configuration file setup, and no configuration file is supplied with the probes. The logic analyzer Buses/Signals setup dialog will allow you to assign descriptive labels to each analyzer channel that associate each channel with the particular DRAM and DRAM signal being probed.

Configuration files are provided with the Keysight B4621A decoder and B4622A protocol compliance software.

Configuration files will also set up the DDR bus decoder, trigger tool, and other software tools.

To save a configuration file

After you set up the logic analyzer, it is strongly recommended that you save the configuration.

To save your work, select **File>Save As...** and save the configuration as an ALA format file.

ALA format configuration files are more complete and efficient than XML format configuration files. See the logic analyzer online help for more information on these formats.

Keysight N5413A DDR2 Compliance Test Application for Infiniium 54850, 80000, and 90000 Series Oscilloscopes

This software performs automated compliance testing of clock jitter, electrical and timing measurements in accordance to JEDEC specifications.

4 Characteristics, Regulatory, and Safety Information

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics.

Table 7 Electrical Characteristics (W2631A/B, W2632A, W2633A/B, W2634A)

Electrical Characteristics	Values
Operating Transfer Rate	800 Mb/s
Bandwidth (f-3dB)	1 GHz
Rise time	350 ps
Input Impedance	
- with Logic Cables Attached	20k Ω
- with Infiniimax Oscilloscope Probe Attached	25k Ω

Table 8 Environmental Characteristics (Operating)

Environmental Characteristics	Values
Temperature	20° to + 30° C (+68° to +86° F)
Altitude	4,600 m (15,000 ft)
Humidity	Up to 50% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only.

Table 9 Inputs and Outputs

Inputs and Outputs	Values
To interposer	Memory bus signals from target system
From interposer	High-density connectors for Keysight logic analyzer cards in an Keysight 16900 Series logic analysis system and for an oscilloscope

Input Impedance

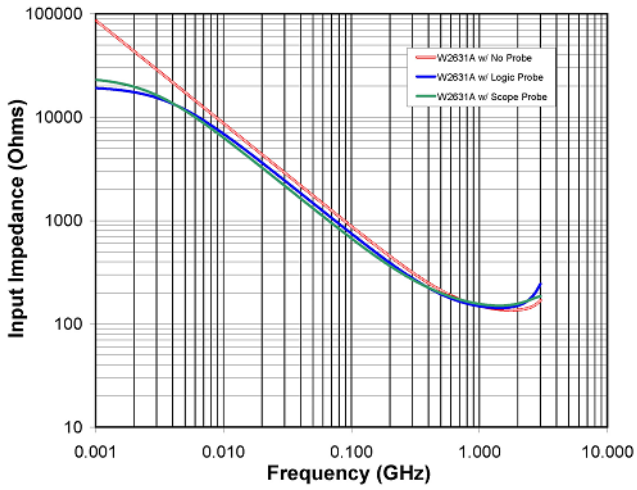

Figure 20 Input Impedance of W2630 Series Probes (with and without instrument probe connections)

NOTES: Logic probe connection made using either the E5384A, E5826A, or E5827A Probe Cables. Oscilloscope probe connection made using the Infiniimax N5425A ZIF Probe with the N5426A tip attached.

Load Model

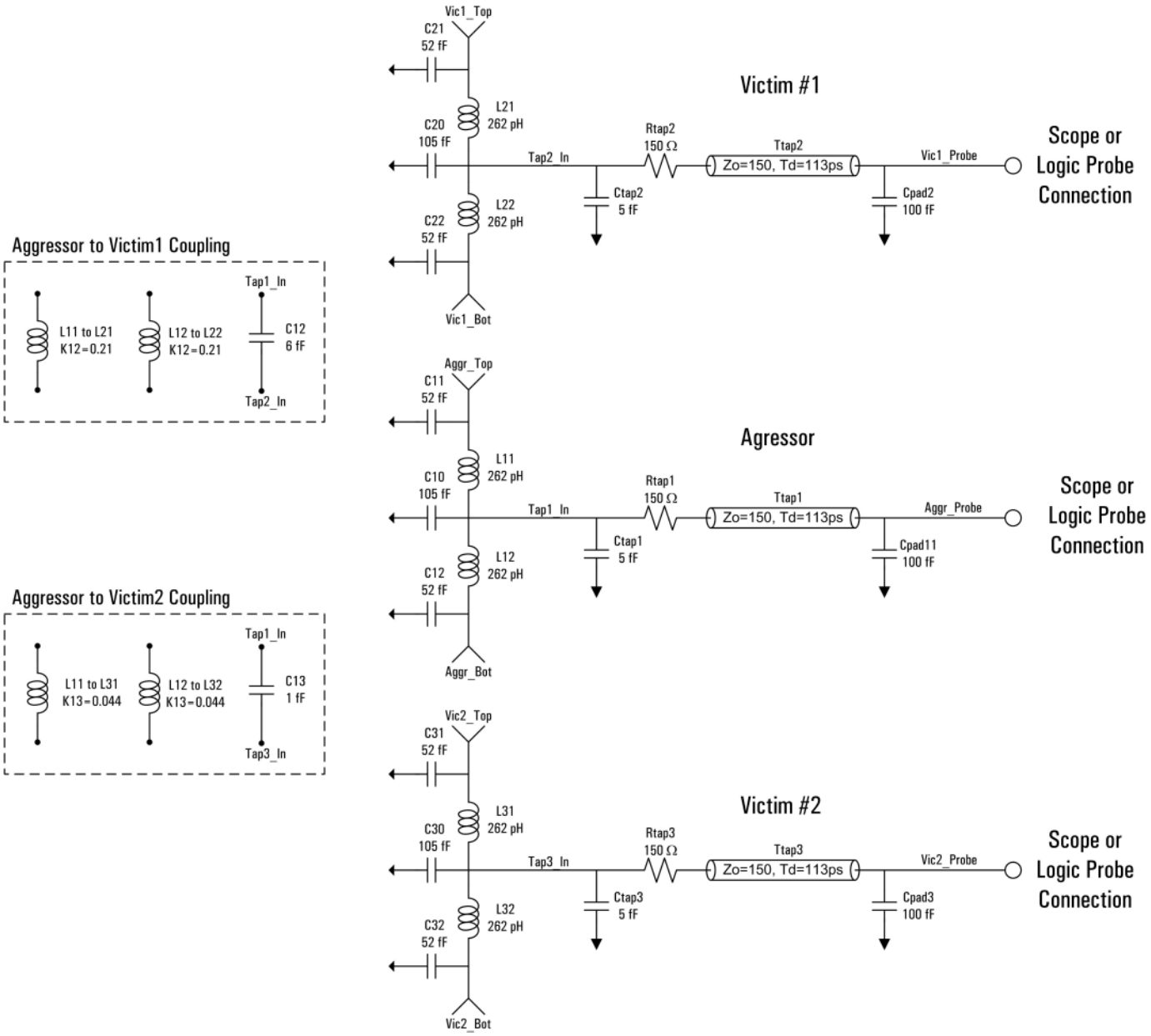

Figure 21 Load Model of W2631A, W2631B, W2632A, W2633A, W2633B, and W2634A Probes (not showing instrument load)

SPICE Deck of Load Model

Without Probe

```
*************************************************************************************************
*** Equivalent Load Model : W2631A/B, W2632A, W2633A/B, and W2634A DDR2 Interposer Probes with No Probe
*** June 2007
*** Rev001
***
*** This SPICE subcircuit models the input impedance of the W2631A, W2632A, W2633 and W2634A DDR2
*** interposer probes. This models the effect of the probe loading on the system.
*** This is a 3-line model which includes mutual inductive and capacitive coupling from
*** one aggressing line to two adjacent victim pins (K12 & K13).
*** This model is accurate up to 3GHz for input impedance simulations.
***
*** Port Description:
***
*** Aggr_Top = Top pad of the interposer for the aggressor line
*** Aggr_Bot = Bottom pad of the interposer for the aggressor line
*** Aggr_Probe = Probe pad along perimeter of the interposer for the aggressor line
*** Vic1_Top = Top pad of the interposer for the Victim #1 line (K12, C12)
*** Vic1_Bot = Bottom pad of the interposer for the Victim #1 line (K12, C12)
*** Vic1_Probe = Probe pad along perimeter of the interposer for the Victim #1 line (13)
*** Vic2_Top = Top pad of the interposer for the Victim #2 line (K12, C12)
*** Vic2_Bot = Bottom pad of the interposer for the Victim #2 line (K12, C12)
*** Vic2_Probe = Probe pad along perimeter of the interposer for the Victim #2 line (13)
***
*** NOTE: The probe ground is assumed to be ideal and is labeled node 0
*** NOTE: K23, C23 is negligible
***
*** This model is used to simulate the load of the interposer with no logic analyzer
*** or oscilloscope attached.
*************************************************************************************************

.subckt W2631_RevA1_Model_NoProbe_SUBCKT
+ Aggr_Top Aggr_Bot Aggr_Probe
+ Vic1_Top Vic1_Bot Vic1_Probe
+ Vic2_Top Vic2_Bot Vic2_Probe

.param Zint=50
.param Tint='(169p)*0.062'
.param Lint='Zint*Tint'
.param Cint='Tint/Zint'
.param K12=0.21
.param K13=0.044
.param C12=6f
.param C13=1f
.param Rtap=150
.param Ctap=5f
.param Ztap=75
.param Ttap='(169p)*0.67'
.param Cpad1=100f

CC10 0 Tap1_In C='Cint/2'
CC11 0 Aggr_Top C='Cint/4'
CC12 0 Aggr_Bot C='Cint/4'
CC20 0 Tap2_In C='Cint/2'
CC21 0 Vic1_Top C='Cint/4'
CC22 0 Vic1_Bot C='Cint/4'
CC30 0 Tap3_In C='Cint/2'
CC31 0 Vic2_Top C='Cint/4'
CC32 0 Vic2_Bot C='Cint/4'
CCcouple12 Tap2_In Tap1_In C=C12
CCcouple13 Tap3_In Tap1_In C=C13
CCpad1 0 Aggr_Probe C=Cpad1
CCpad2 0 Vic1_Probe C=Cpad1
CCpad3 0 Vic2_Probe C=Cpad1
CCtap1 0 Tap1_In C=Ctap
CCtap2 0 Tap2_In C=Ctap
CCtap3 0 Tap3_In C=Ctap
LL11 Aggr_Top Tap1_In 'Lint/2'
LL12 Tap1_In Aggr_Bot 'Lint/2'
LL21 Vic1_Top Tap2_In 'Lint/2'
LL22 Tap2_In Vic1_Bot 'Lint/2'
LL31 Vic2_Top Tap3_In 'Lint/2'
LL32 Tap3_In Vic2_Bot 'Lint/2'
```

```
RRtap1 Tap1_In _net4577 Rtap
RRtap2 Tap2_In _net4578 Rtap
RRtap3 Tap3_In _net4540 Rtap
TTtap1 _net4577 Aggr_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap2 _net4578 Vic1_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap3 _net4540 Vic2_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'

.ends W2631_RevA1_Model_NoProbe_SUBCKT
```

With Logic Probe

```
*************************************************************************************************
*** Equivalent Load Model : W2631A/B, W2632A, W2633A/B, and W2634A DDR2 Interposer Probes with Logic Probe Attached
*** June 2007
*** Rev001
***
*** This SPICE subcircuit models the input impedance of the W2631A, W2632A, W2633 and W2634A DDR2
*** interposer probes. This models the effect of the probe loading on the system.
*** This is a 3-line model which includes mutual inductive and capacitive coupling from
*** one aggressing line to two adjacent victim pins (K12 & K13).
*** This model is accurate up to 3GHz for input impedance simulations.
***
*** Port Description:
*** Aggr_Top = Top pad of the interposer for the aggressor line
*** Aggr_Bot = Bottom pad of the interposer for the aggressor line
*** Aggr_Probe = Probe pad along perimeter of the interposer for the aggressor line
*** Vic1_Top = Top pad of the interposer for the Victim #1 line (K12, C12)
*** Vic1_Bot = Bottom pad of the interposer for the Victim #1 line (K12, C12)
*** Vic1_Probe = Probe pad along perimeter of the interposer for the Victim #1 line (K13, C13)
*** Vic2_Top = Top pad of the interposer for the Victim #2 line (K12, C12)
*** Vic2_Bot = Bottom pad of the interposer for the Victim #2 line (K12, C12)
*** Vic2_Probe = Probe pad along perimeter of the interposer for the Victim #2 line (K13, C13)
***
*** NOTE: The probe ground is assumed to be ideal and is labeled node 0
*** NOTE: K23, C23 is negligible
***
*** This model is used to simulate the load of the interposer with a logic analyzer attached
*** using either the E5384A, E5826A, or E5827A adapter cables.
*************************************************************************************************

.subckt W2631_RevA1_Model_LogicProbe_SUBCKT
+ Aggr_Top Aggr_Bot Aggr_Probe
+ Vic1_Top Vic1_Bot Vic1_Probe
+ Vic2_Top Vic2_Bot Vic2_Probe

.param Rtip=20k
.param Ctip=350f
.param Rterm=75
.param Vterm=0.7
.param Zint=50
.param Tint='(169p)*0.062'
.param Lint='Zint*Tint'
.param Cint='Tint/Zint'
.param K12=0.21
.param K13=0.044
.param C12=6f
.param C13=1f
.param Rtap=150
.param Ctap=5f
.param Ztap=75
.param Ttap='(169p)*0.67'
.param Cpad1=100f

CC10 0 Tap1_In C='Cint/2'
CC11 0 Aggr_Top C='Cint/4'
CC12 0 Aggr_Bot C='Cint/4'
CC20 0 Tap2_In C='Cint/2'
CC21 0 Vic1_Top C='Cint/4'
CC22 0 Vic1_Bot C='Cint/4'
CC30 0 Tap3_In C='Cint/2'
CC31 0 Vic2_Top C='Cint/4'
CC32 0 Vic2_Bot C='Cint/4'
CCcouple12 Tap2_In Tap1_In C=C12
CCcouple13 Tap3_In Tap1_In C=C13
CCpad1 0 Aggr_Probe C=Cpad1
CCpad2 0 Vic1_Probe C=Cpad1
CCpad3 0 Vic2_Probe C=Cpad1
```

```
CCtap1 0 Tap1_In C=Ctap
CCtap2 0 Tap2_In C=Ctap
CCtap3 0 Tap3_In C=Ctap
CCtip1 _net4688 Aggr_Probe C=Ctip
CCtip2 _net4697 Vic1_Probe C=Ctip
CCtip3 _net4707 Vic2_Probe C=Ctip
LL11 Aggr_Top Tap1_In 'Lint/2'
LL12 Tap1_In Aggr_Bot 'Lint/2'
LL21 Vic1_Top Tap2_In 'Lint/2'
LL22 Tap2_In Vic1_Bot 'Lint/2'
LL31 Vic2_Top Tap3_In 'Lint/2'
LL32 Tap3_In Vic2_Bot 'Lint/2'
RRtap1 Tap1_In _net4577 Rtap
RRtap2 Tap2_In _net4578 Rtap
RRtap3 Tap3_In _net4540 Rtap
RRterm1 _net4688 _net4689 Rterm
RRterm2 _net4697 _net4699 Rterm
RRterm3 _net4707 _net4708 Rterm
RRtip1 Aggr_Probe _net4688 Rtip
RRtip2 Vic1_Probe _net4697 Rtip
RRtip3 Vic2_Probe _net4707 Rtip
TTtap1 _net4577 Aggr_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap2 _net4578 Vic1_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap3 _net4540 Vic2_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
VVterm1 _net4689 0 Vterm
VVterm2 _net4699 0 Vterm
VVterm3 _net4708 0 Vterm

.ends W2631_RevA1_Model_LogicProbe_SUBCKT
```

With Oscilloscope Probe

```
*************************************************************************************************************
*** Equivalent Load Model : W2631A/B, W2632A, W2633A/B and W2634A DDR2 Interposer Probes with Oscilloscope Probe
*** June 2007
*** Rev001
***
*** This SPICE subcircuit models the input impedance of the W2631A, W2632A, W2633 and W2634A DDR2
*** interposer probes. This models the effect of the probe loading on the system.
*** This is a 3-line model which includes mutual inductive and capacitive coupling from
*** one aggressing line to two adjacent victim pins (K12 & K13).
*** This model is accurate up to 3GHz for input impedance simulations.
***
*** Port Description:
***
*** Aggr_Top = Top pad of the interposer for the aggressor line
*** Aggr_Bot = Bottom pad of the interposer for the aggressor line
*** Aggr_Probe = Probe pad along perimeter of the interposer for the aggressor line
*** Vic1_Top = Top pad of the interposer for the Victim #1 line (K12, C12)
*** Vic1_Bot = Bottom pad of the interposer for the Victim #1 line (K12, C12)
*** Vic1_Probe = Probe pad along perimeter of the interposer for the Victim #1 line (K13, C13)
*** Vic2_Top = Top pad of the interposer for the Victim #2 line (K12, C12)
*** Vic2_Bot = Bottom pad of the interposer for the Victim #2 line (K12, C12)
*** Vic2_Probe = Probe pad along perimeter of the interposer for the Victim #2 line (K13, C13)
***
*** NOTE: The probe ground is assumed to be ideal and is labeled node 0
*** NOTE: K23, C23 is negligible
***
*** This model is used to simulate the load of the interposer with the Keysight N5425A ZIF Probe head
*** with the N5426A ZIF Tip attached and soldered to the observation pads on the interposer.
***
***
*************************************************************************************************************

.subckt W2631_RevA1_Model_ScopeProbe_SUBCKT
+ Aggr_Top Aggr_Bot Aggr_Probe
+ Vic1_Top Vic1_Bot Vic1_Probe
+ Vic2_Top Vic2_Bot Vic2_Probe

.param Zint=50
.param Tint='(169p)*0.062'
.param Lint='Zint*Tint'
.param Cint='Tint/Zint'
.param K12=0.21
.param K13=0.044
.param C12=6f
.param C13=1f
```

```
.param Rtap=150
.param Ctap=5f
.param Ztap=75
.param Ttap='(169p)*0.67'
.param Cpad1=100f

CC1 _net4933 _net4991 C=14.75fF
CC10 0 Tap1_In C='Cint/2'
CC11 0 Aggr_Top C='Cint/4'
CC12 0 Aggr_Bot C='Cint/4'
CC2 _net4941 _net4991 C=6.3fF
CC20 0 Tap2_In C='Cint/2'
CC21 0 Vic1_Top C='Cint/4'
CC22 0 Vic1_Bot C='Cint/4'
CC30 0 Tap3_In C='Cint/2'
CC31 0 Vic2_Top C='Cint/4'
CC32 0 Vic2_Bot C='Cint/4'
CC33 _net5160 _net5186 C=6.3fF
CC34 _net5152 _net5186 C=14.75fF
CC35 _net5309 _net5335 C=6.3fF
CC36 _net5301 _net5335 C=14.75fF
CCcouple12 Tap2_In Tap1_In C=C12
CCcouple13 Tap3_In Tap1_In C=C13
CCn1 _net4948 _net5008 C=556.5fF
CCn2 _net4963 _net5008 C=40.93fF
CCn3 _net5182 _net5190 C=40.93fF
CCn4 _net5167 _net5190 C=556.5fF
CCn5 _net5331 _net5339 C=40.93fF
CCn6 _net5316 _net5339 C=556.5fF
CCp1 _net4951 _net5031 C=556.5fF
CCp2 _net4960 _net5031 C=40.93fF
CCp3 _net5179 _net5191 C=40.93fF
CCp4 _net5170 _net5191 C=556.5fF
CCp5 _net5328 _net5340 C=40.93fF
CCp6 _net5319 _net5340 C=556.5fF
CCpad1 0 Aggr_Probe C=Cpad1
CCpad2 0 Vic1_Probe C=Cpad1
CCpad3 0 Vic2_Probe C=Cpad1
CCtap1 0 Tap1_In C=Ctap
CCtap2 0 Tap2_In C=Ctap
CCtap3 0 Tap3_In C=Ctap
LL1 _net4933 _net4936 1.356nH
LL11 Aggr_Top Tap1_In 'Lint/2'
LL12 Tap1_In Aggr_Bot 'Lint/2'
LL2 _net4941 _net4942 345.2pH
LL21 Vic1_Top Tap2_In 'Lint/2'
LL22 Tap2_In Vic1_Bot 'Lint/2'
LL31 Vic2_Top Tap3_In 'Lint/2'
LL32 Tap3_In Vic2_Bot 'Lint/2'
LL33 _net5160 _net5161 345.2pH
LL34 _net5152 _net5155 1.356nH
LL35 _net5309 _net5310 345.2pH
LL36 _net5301 _net5304 1.356nH
LLn1 _net4948 _net4946 3.815nH
LLn2 _net4963 _net4966 5.731nH
LLn3 _net5182 _net5185 5.731nH
LLn4 _net5167 _net5165 3.815nH
LLn5 _net5331 _net5334 5.731nH
LLn6 _net5316 _net5314 3.815nH
LLom _net5031 0 1uH
LLom2 _net5038 0 2nH
LLom3 _net5193 0 2nH
LLom4 _net5191 0 1uH
LLom5 _net5342 0 2nH
LLom6 _net5340 0 1uH
LLp1 _net4951 _net4954 3.815nH
LLp2 _net4960 _net4958 5.731nH
LLp3 _net5179 _net5177 5.731nH
LLp4 _net5170 _net5173 3.815nH
LLp5 _net5328 _net5326 5.731nH
LLp6 _net5319 _net5322 3.815nH
RR1 _net4936 _net5008 948.2
RR2 _net4942 _net5008 36.88
RR3 _net5161 _net5190 36.88
RR4 _net5155 _net5190 948.2
RR5 _net5310 _net5339 36.88
RR6 _net5304 _net5339 948.2
RRn1 _net4946 _net5031 38.32
```

```
RRn2 _net4966 _net5031 30.4
RRn3 _net5008 _net5031 25kOhm
RRn4 _net5190 _net5191 25kOhm
RRn5 _net5185 _net5191 30.4
RRn6 _net5165 _net5191 38.32
RRn7 _net5339 _net5340 25kOhm
RRn8 _net5334 _net5340 30.4
RRn9 _net5314 _net5340 38.32
RRom _net5038 _net5031 250
RRom1 _net5193 _net5191 250
RRom2 _net5342 _net5340 250
RRp1 _net4954 _net4991 38.32
RRp2 _net4958 _net4991 30.4
RRp3 _net5031 _net4991 25kOhm
RRp4 _net5191 _net5186 25kOhm
RRp5 _net5177 _net5186 30.4
RRp6 _net5173 _net5186 38.32
RRp7 _net5340 _net5335 25kOhm
RRp8 _net5326 _net5335 30.4
RRp9 _net5322 _net5335 38.32
RRtap1 Tap1_In _net4577 Rtap
RRtap2 Tap2_In _net5076 Rtap
RRtap3 Tap3_In _net5224 Rtap
RRtipn 0 _net5008 64.35
RRtipn1 0 _net5190 64.35
RRtipn2 0 _net5339 64.35
RRtipp Aggr_Probe _net4991 64.35
RRtipp1 Vic1_Probe _net5186 64.35
RRtipp2 Vic2_Probe _net5335 64.35
TTtap1 _net4577 Aggr_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap2 _net5076 Vic1_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap3 _net5224 Vic2_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'

.ends W2631_RevA1_Model_ScopeProbe_SUBCKT
```

Safety Notices for the E5384A, E5826A, and E5827A Cable Adapters

Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

Do not attempt to clean this product.

Safety Symbols

Safety Symbol	Description
	"Caution" or "Warning" risk of danger marked on product. See "Safety Notices" on page 2 and refer to this manual for a description of the specific danger.
	Hazardous voltage symbol.
	Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

Regulatory Notices

WEEE Compliance

Safety Symbol	Description
	This product complies with the WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/electronic product in domestic household waste. *Product Category: With reference to the equipment types in the WEEE Directive Annex I, this product is classed as a "Monitoring and Control Instrumentation" product.* **Do not dispose in domestic household waste. To return unwanted products, contact your local Keysight office, or see** "www.keysight.com" for more information.

China RoHS

W2631A, W2631B, W2632A, W2633A, W2633B, W2634A, E5384A, E5826A, and E5827A

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