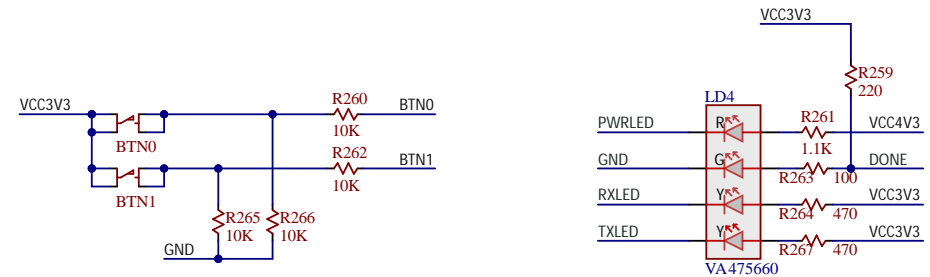
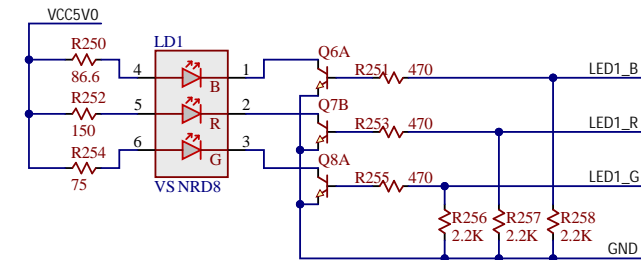
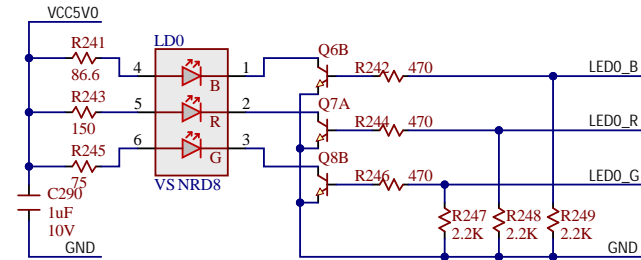


Sheet

Circuit

1. LEDs, Buttons
2. PMOD Ports
3. SYZGY Ports
4. Ethernet and SD Card
5. USB OTG
6. FPGA Configuration
7. DDR and MIO Banks
8. FPGA Banks
9. FPGA Power
10. DDR3L Memory
11. DDR3L Termination
12. Platform MCU
13. Power Regulation
14. Power Regulation
15. Power Regulation and Sequencer

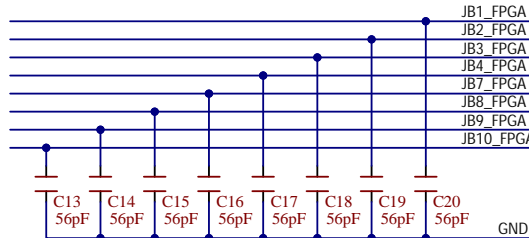
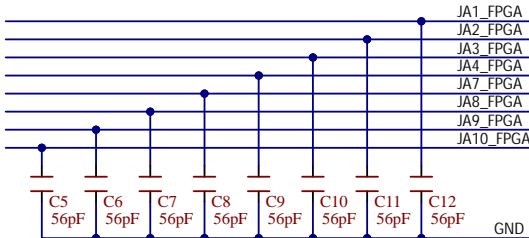
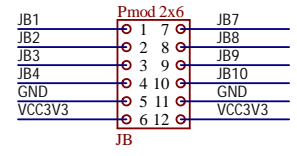
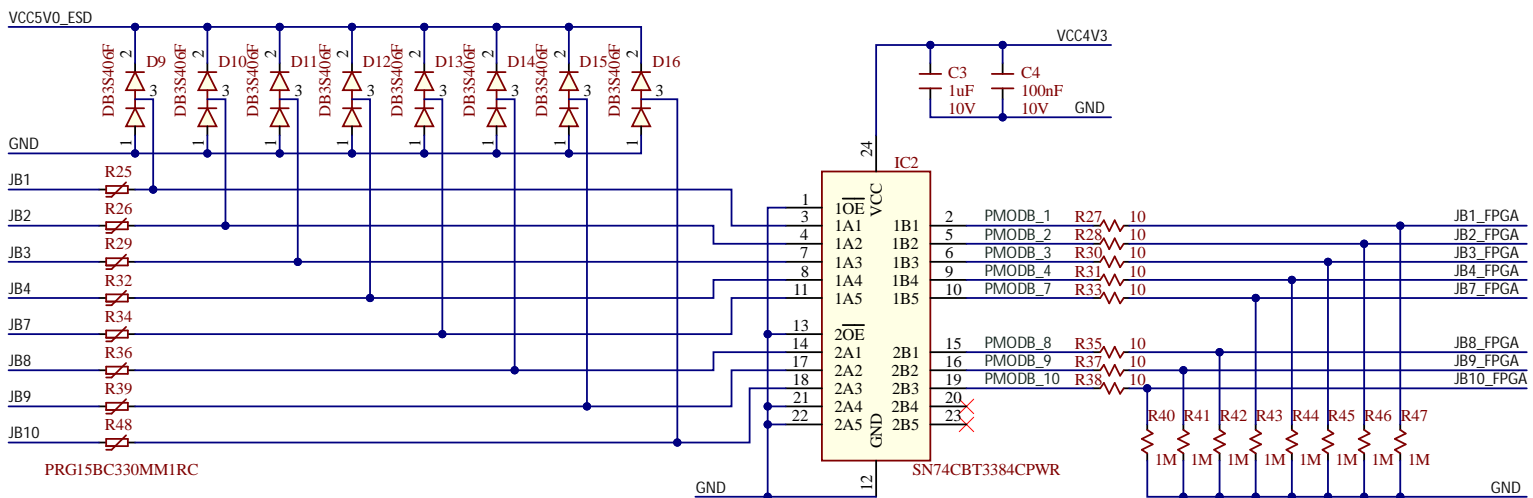
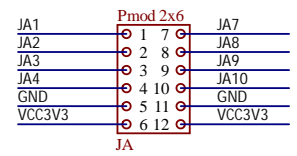
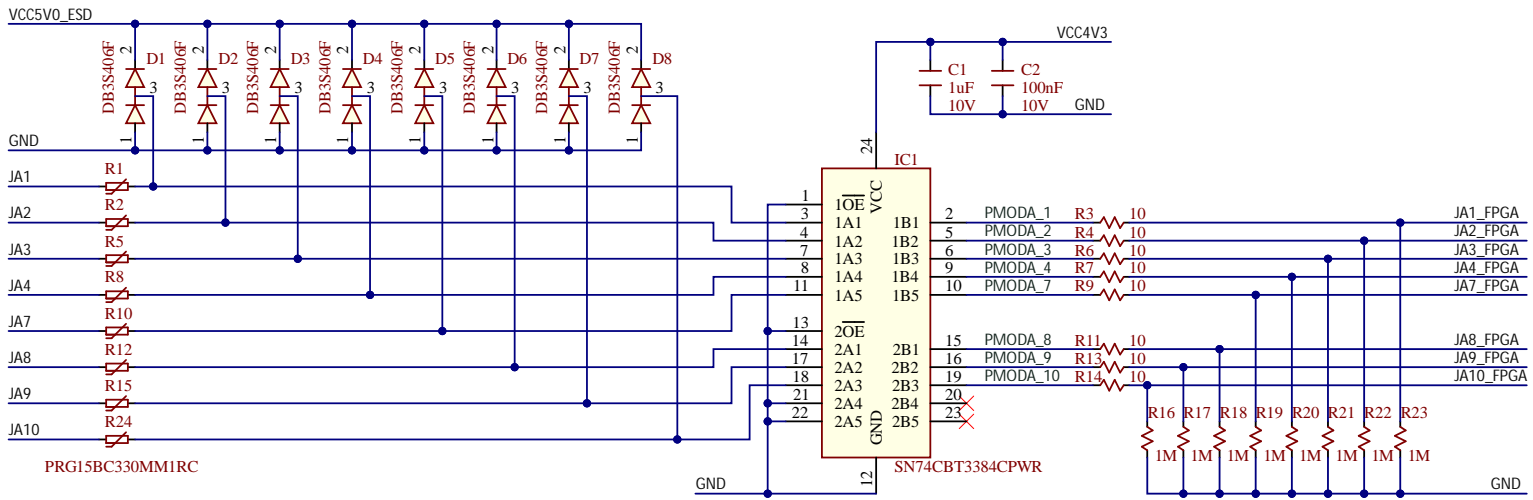


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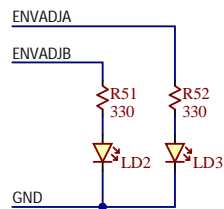
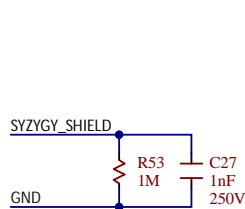
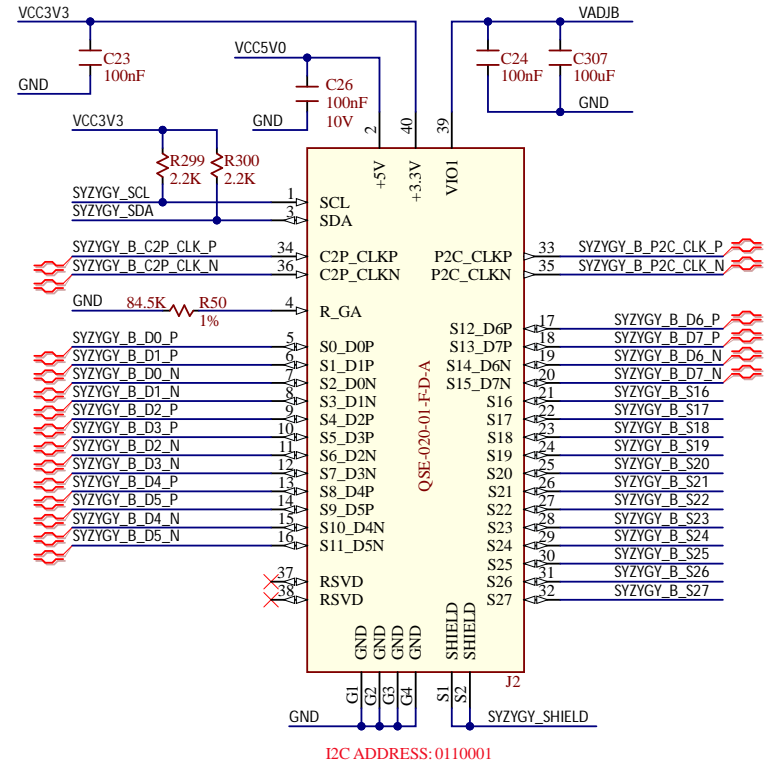
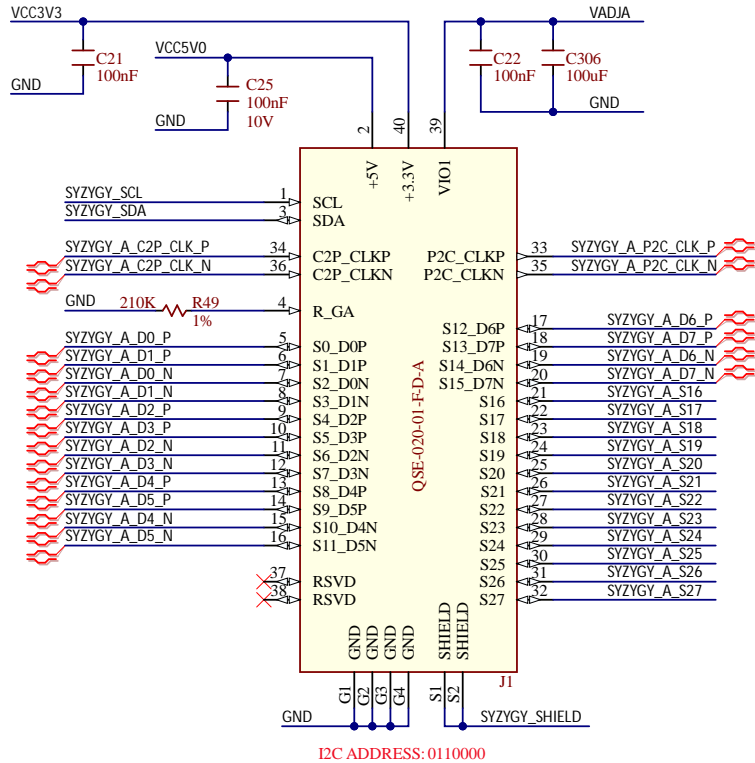
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Foot
F1
Foot
F2

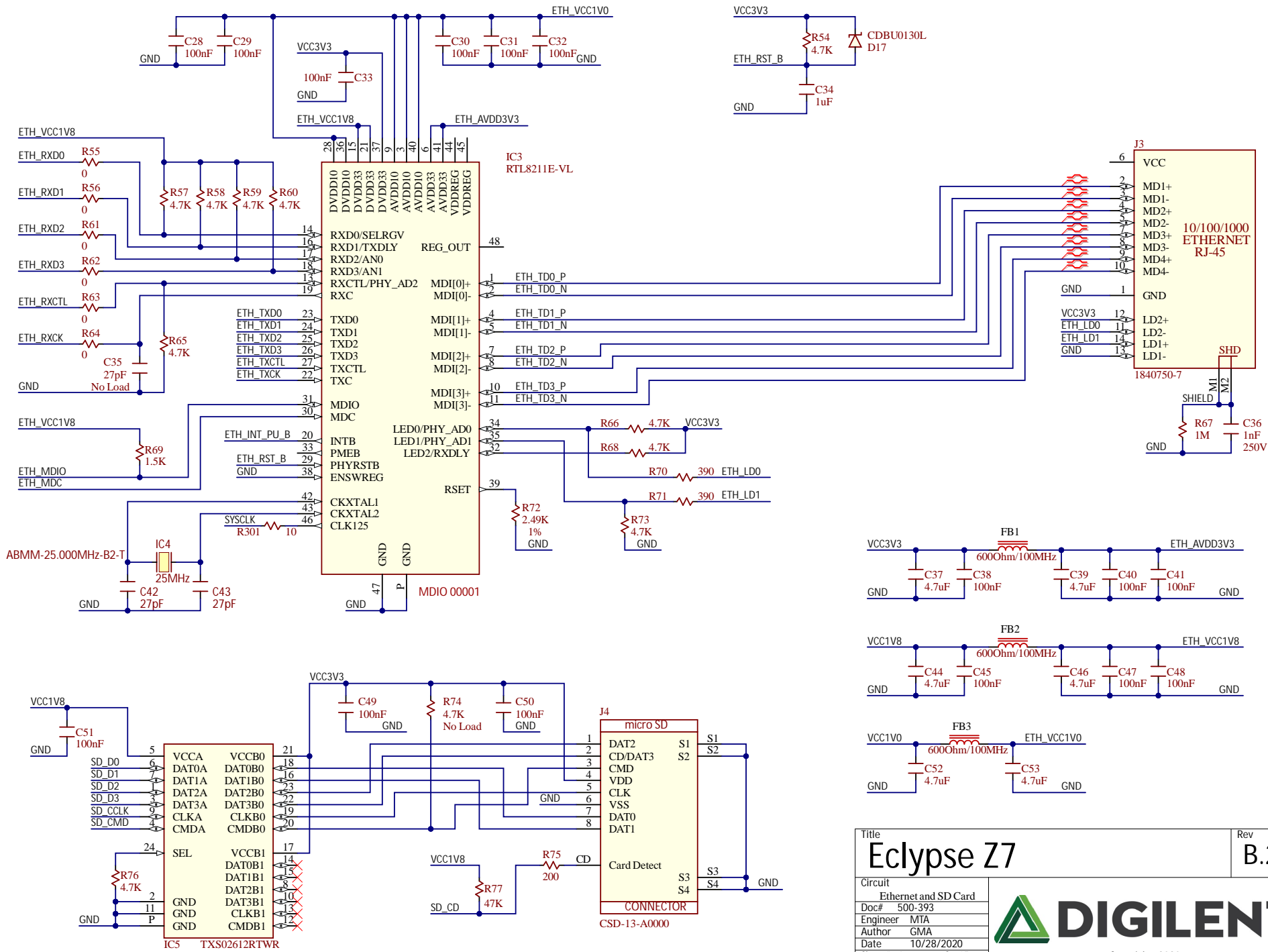
Title Eclipse Z7		Rev B.2
Circuit LEDs, Buttons	Doc# 500-393	 Copyright 2020
Engineer MTA	Author GMA	
Date 10/28/2020	Sheet# 1 out of 15	
Foot		
Foot		



Title		Rev
Eclipse Z7		B.2
Circuit		
Pmod Ports		
Doc#	500-393	
Engineer	MTA	
Author	GMA	
Date	10/28/2020	
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		Copyright 2020

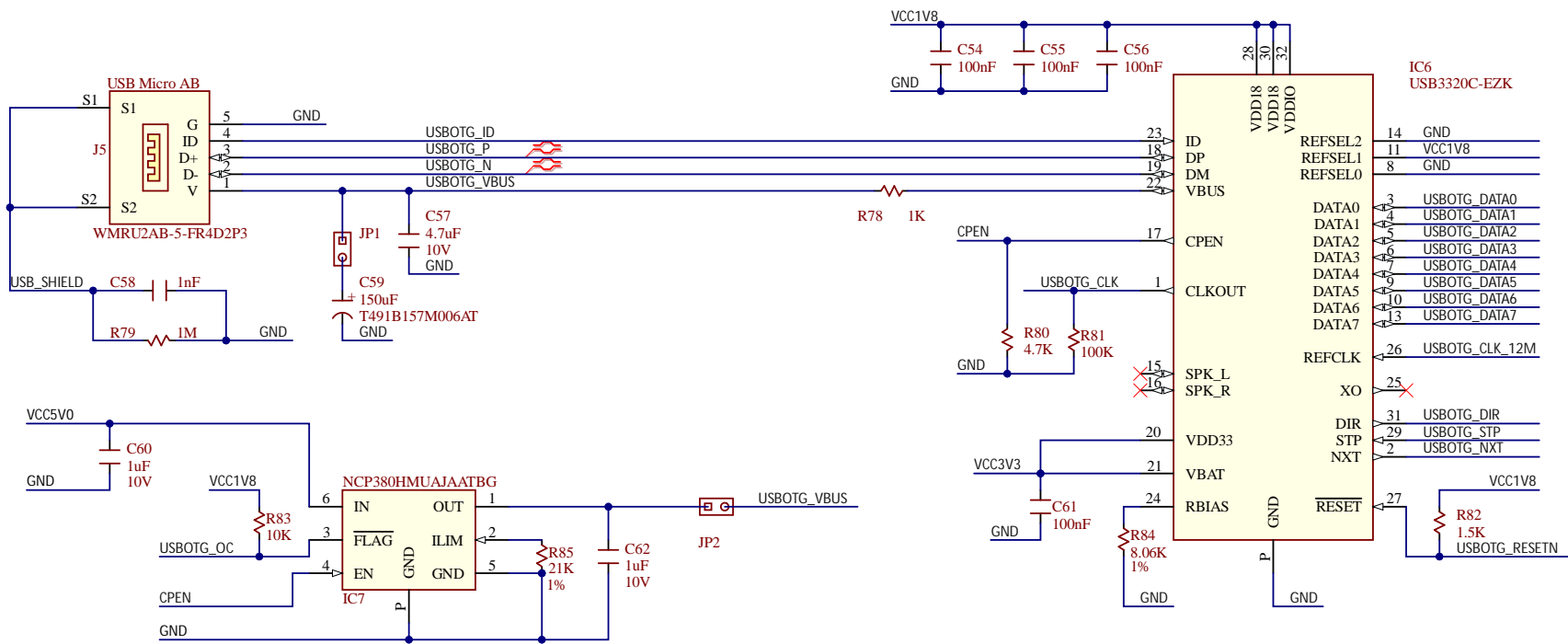


Title Eclipse Z7		Rev B.2
Circuit SYZYGY Ports		
Doc# 500-393		
Engineer MTA		
Author GMA		
Date 10/28/2020		
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		Copyright 2020



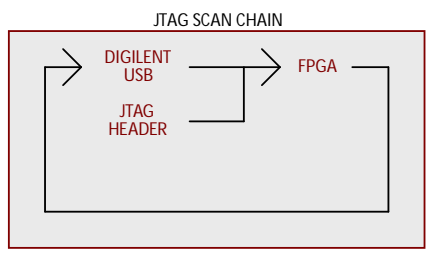
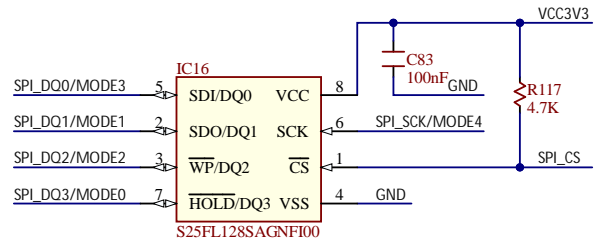
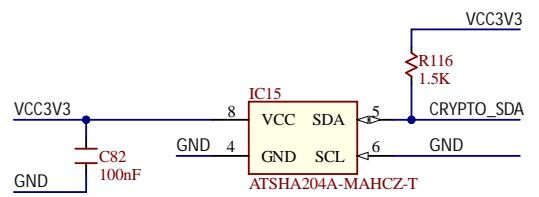
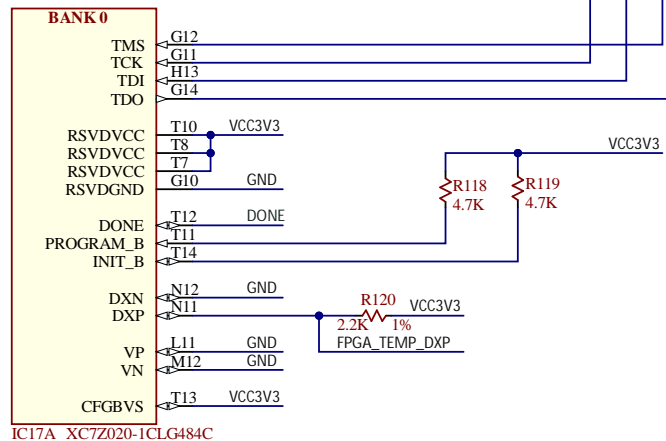
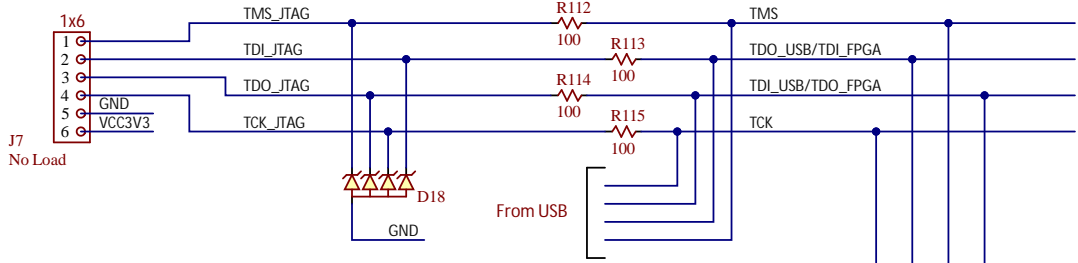
Title		Rev	
Eclipse Z7		B.2	
Circuit			
Ethernet and SD Card			
Doc#	500-393	Author	GMA
Engineer	MTA	Date	10/28/2020
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Title		Eclipse Z7		Rev		B.2	
Circuit		UST OTG		Doc#		500-393	
		Engineer		Author		GMA	
		Date		Sheet#		5 out of 15	
				Copyright		2020	

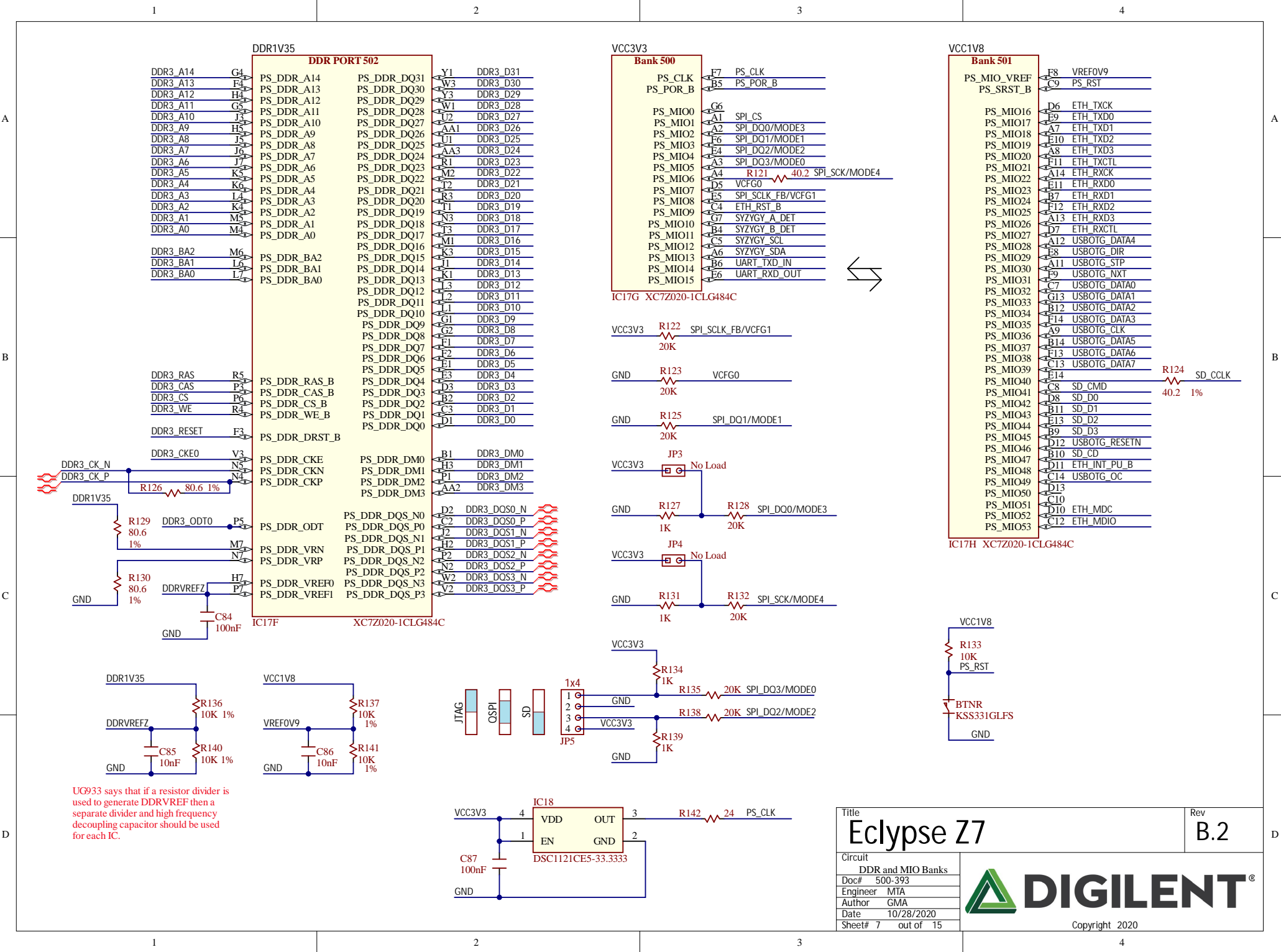




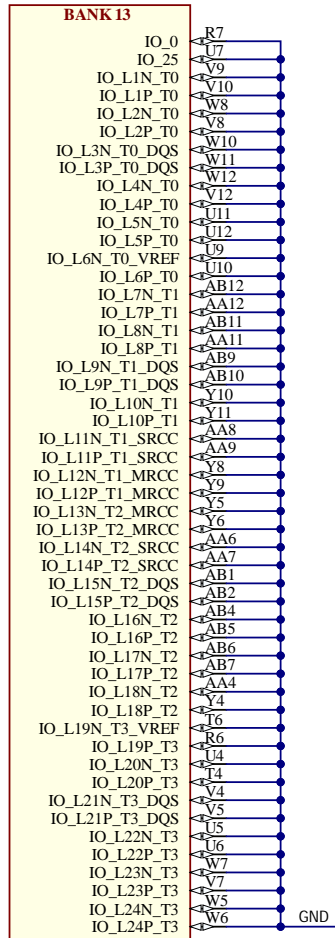
Title		Rev
Eclypse Z7		B.2
Circuit		
FPGA Configuration		
Doc#	500-393	
Engineer	MTA	
Author	GMA	
Date	10/28/2020	
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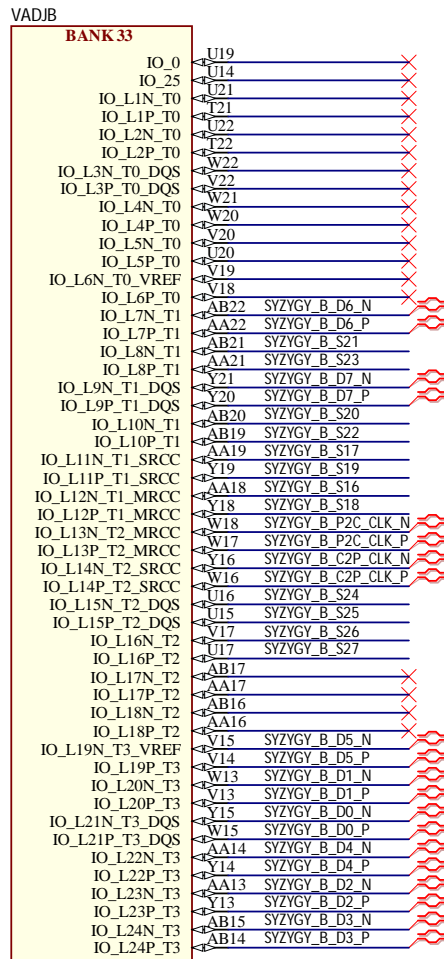
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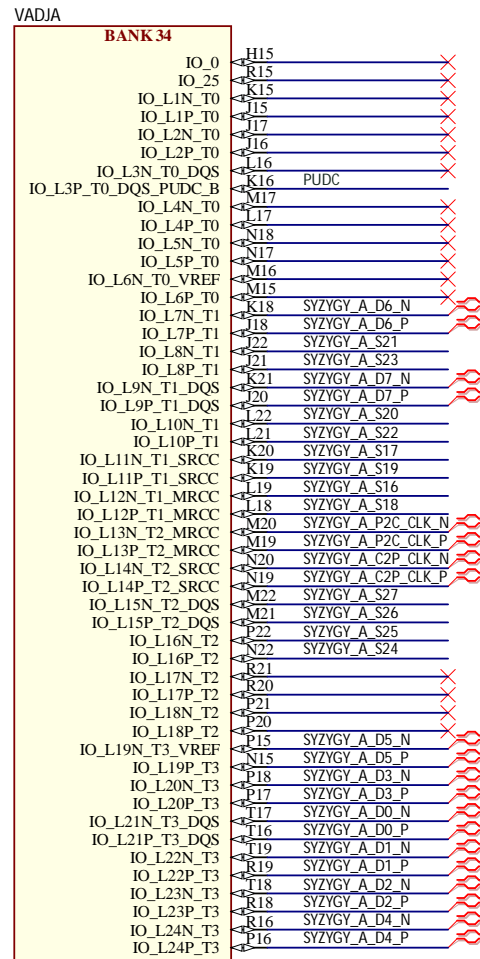
Title		Rev	
Eclipse Z7		B.2	
Circuit			
DDR and MIO Banks			
Doc# 500-393			
Engineer MTA			
Author GMA			
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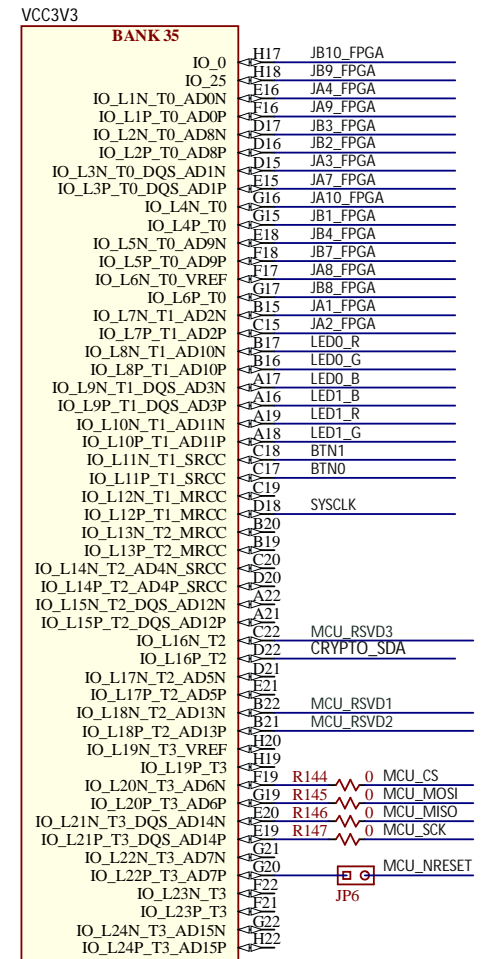
IC17B XC7Z020-1CLG484C



IC17C XC7Z020-1CLG484C

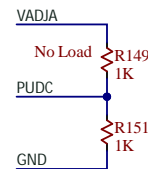
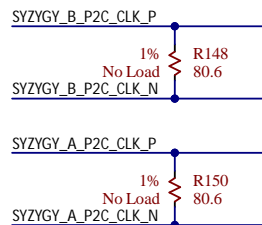


IC17D XC7Z020-1CLG484C



IC17E XC7Z020-1CLG484C

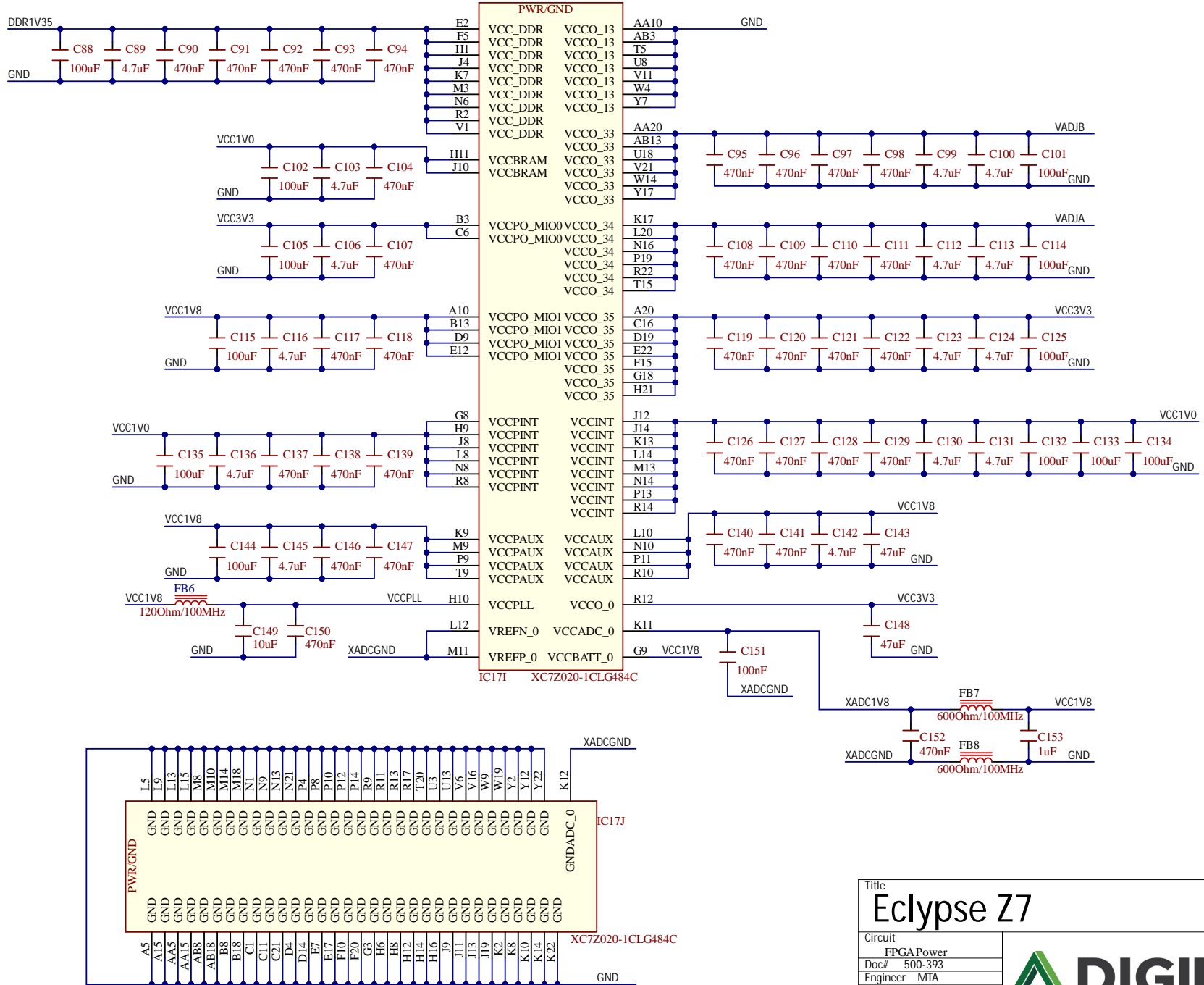
UG933 says to connect the I/O pins of an unused bank to the same potential as the VCC0 pins of that bank.



Title		Rev	
Eclipse Z7		B.2	
Circuit			
FPGA Banks			
Doc#	500-393		
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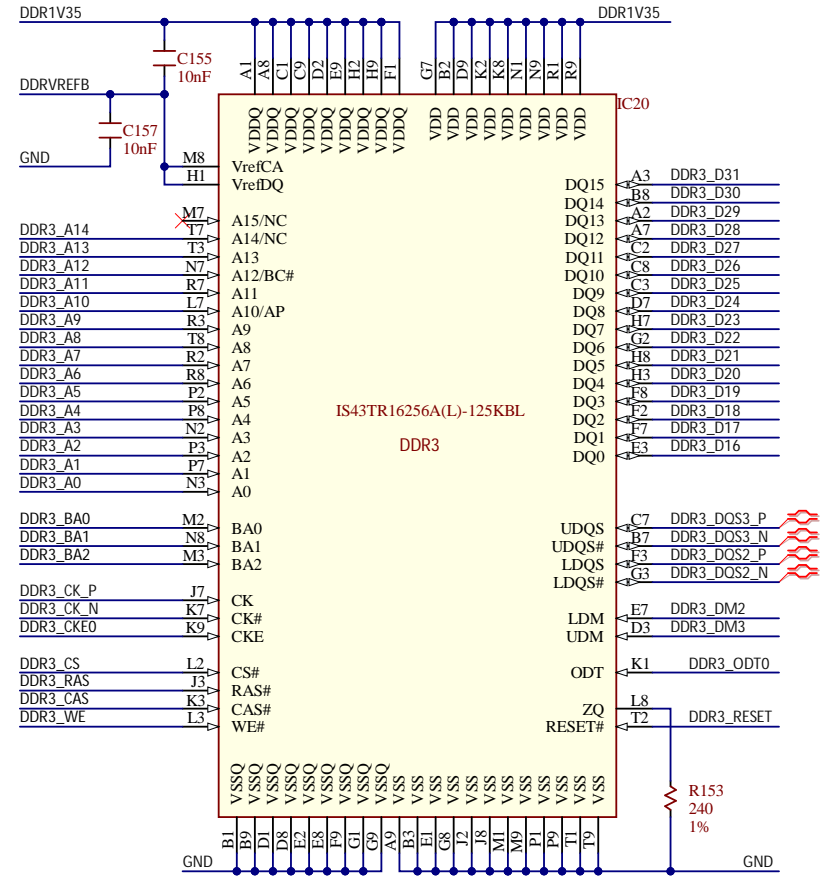
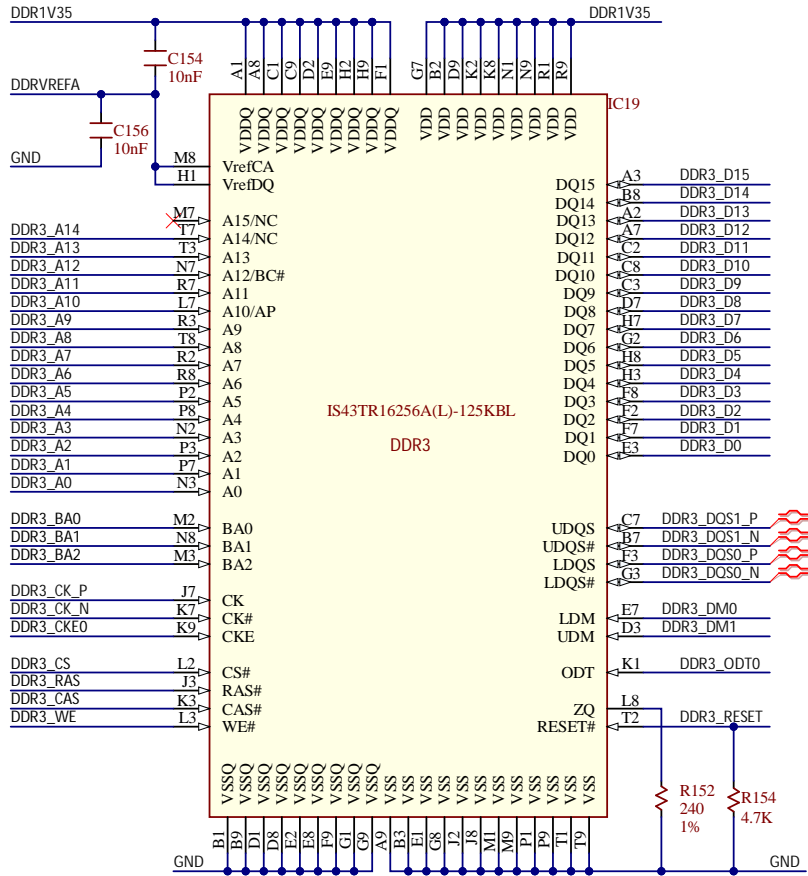
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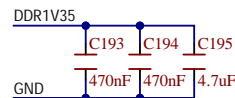
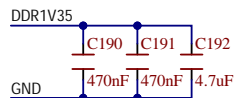
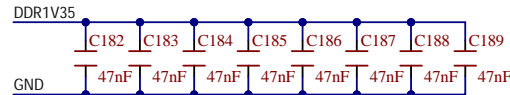
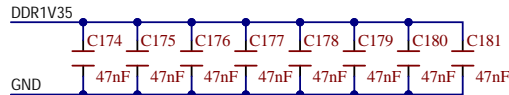
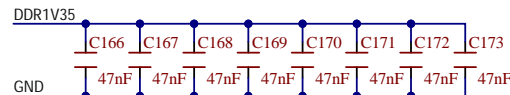
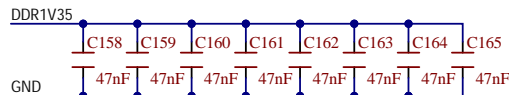
Title		Rev
Eclypse Z7		B.2
Circuit		
FPGA Power		
Doc# 500-393		
Engineer MTA		
Author GMA		
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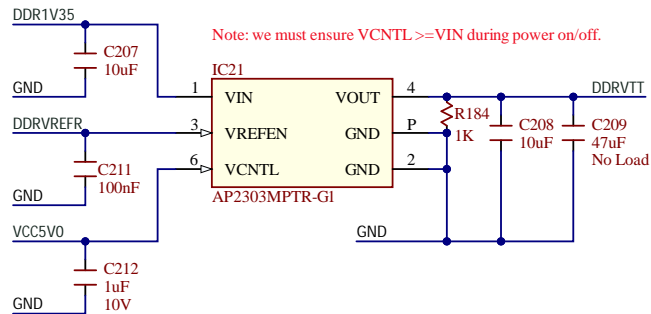
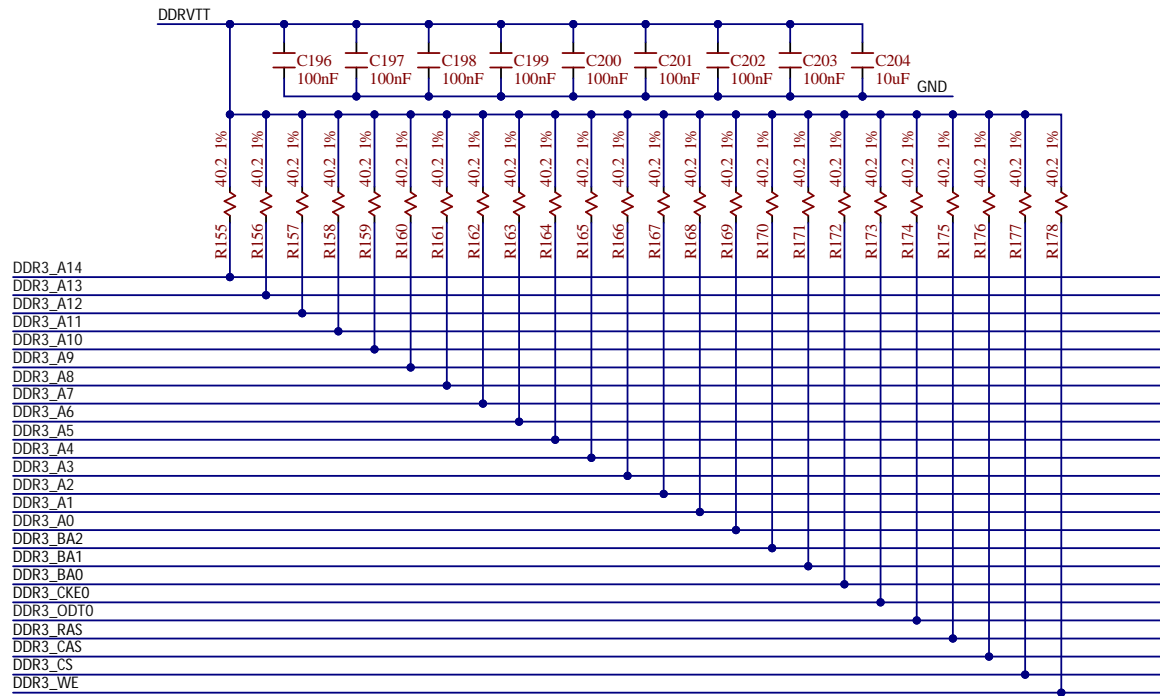
NOTE: Please select Micron MT41K256M16 RE-125 as the Memory Part in the Vivado DDR Configuration.



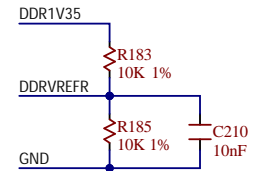
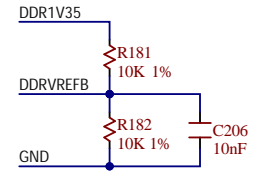
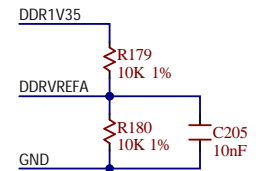
Title		Rev	
Eclypse Z7		B.2	
Circuit			
DDR3L Memory			
Doc# 500-393			
Engineer MTA			
Author GMA			
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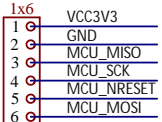
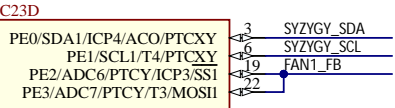
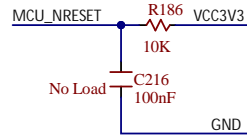
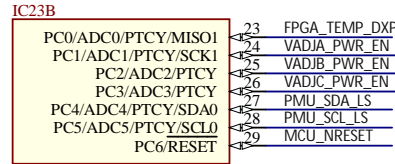
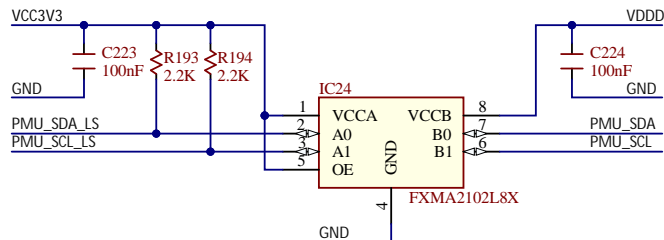
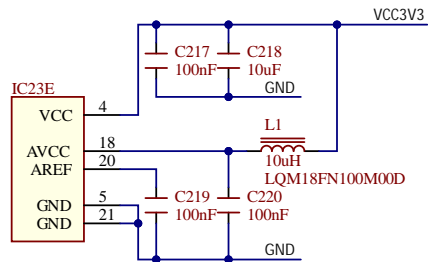
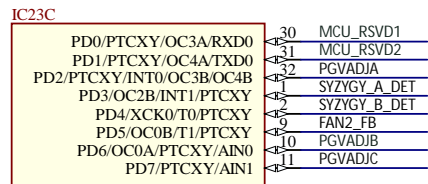
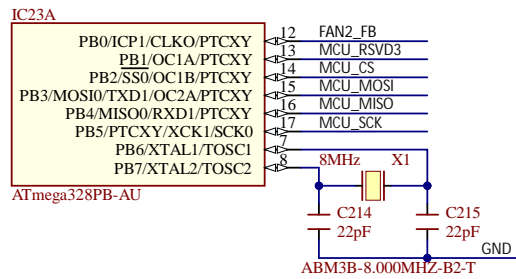
UG933 says that if a resistor divider is used to generate DDRVREF then a separate divider and high frequency decoupling capacitor should be used for each IC.



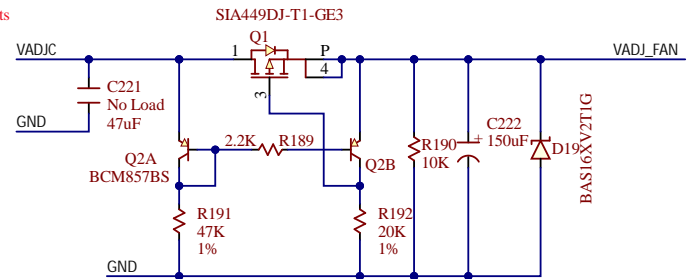
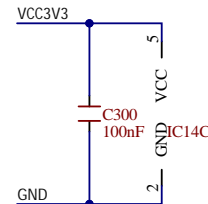
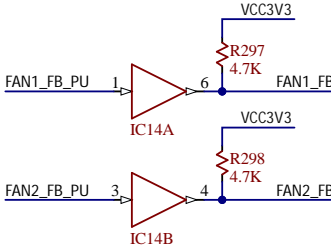
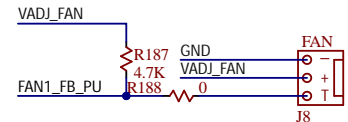
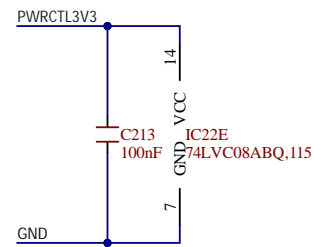
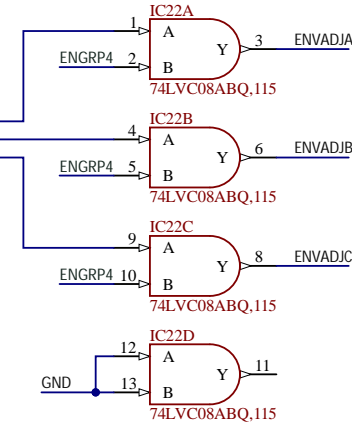
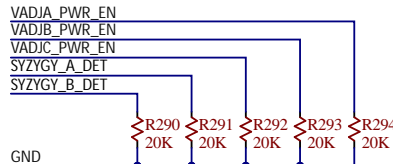
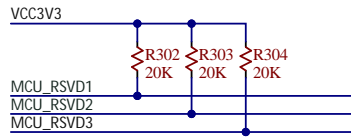
Title Eclipse Z7		Rev B.2
Circuit DDR3L Termination		
Doc# 500-393		
Engineer MTA		
Author GMA		
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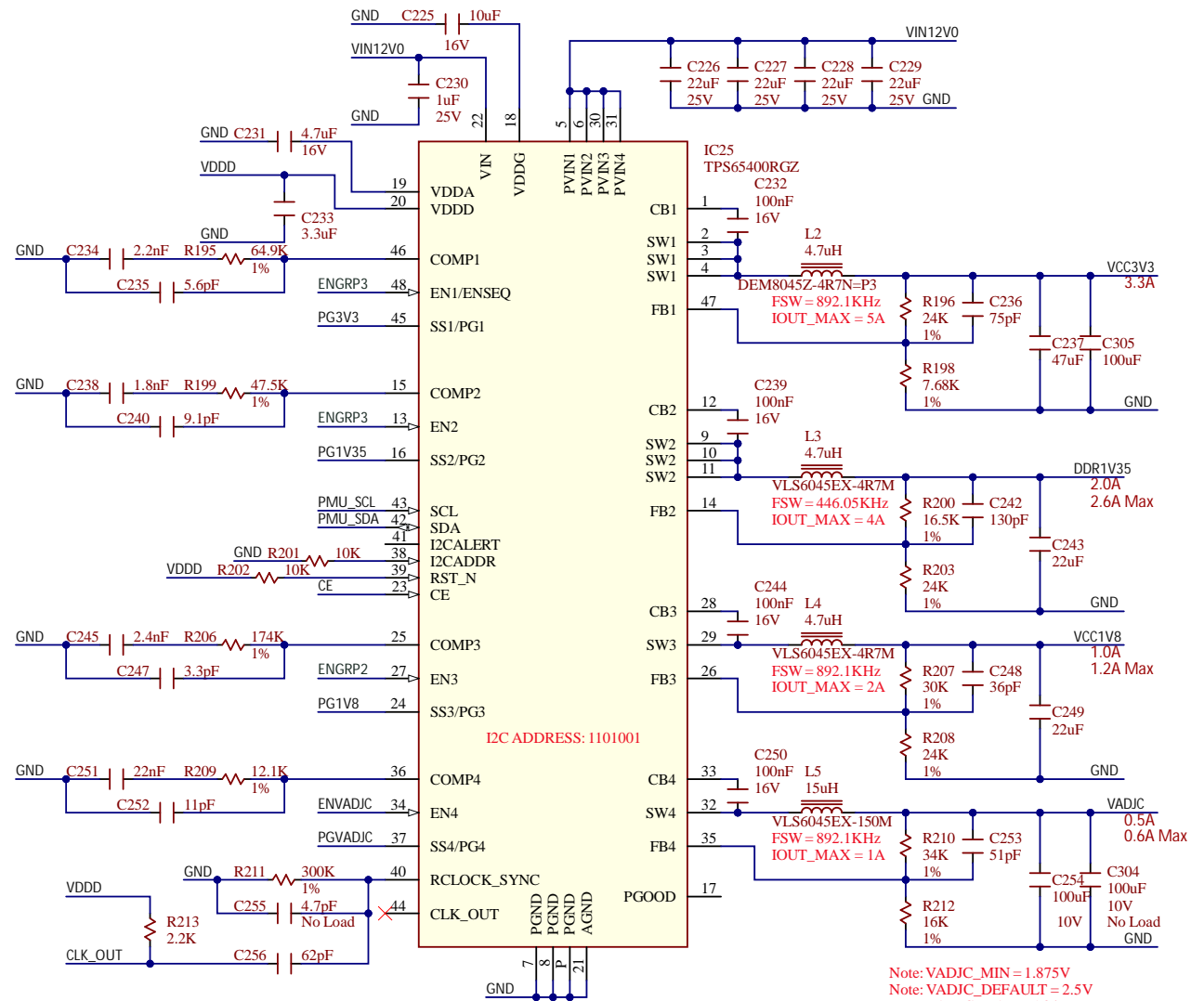
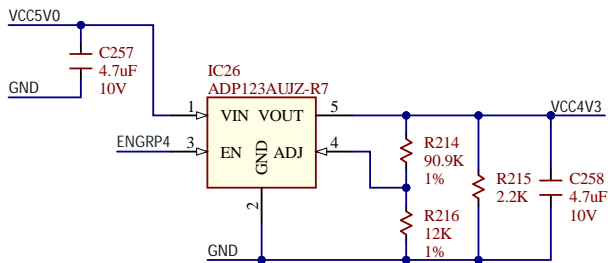
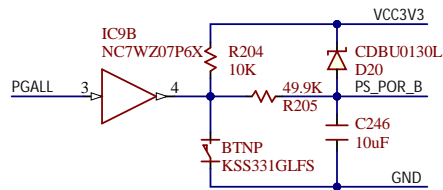
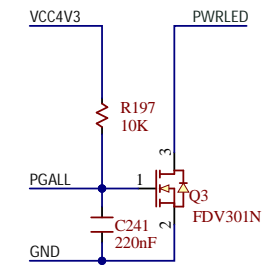


J9
 No Load
 Program/Debug using MPLAB SNAP Debugger
 Pin 2 of the SNAP connects to pin 1 on the board
 SNAP Pinout: <http://microchipdeveloper.com/pickit4:interface-pinouts>



Title		Rev	
Eclypse Z7		B.2	
Circuit			
Platform MCU			
Doc# 500-393			
Engineer MTA			
Author GMA			
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ISENSE_GAIN = 10A/V for all channels
 TON_RAMP_RATE = 0.25V/ms for all channels

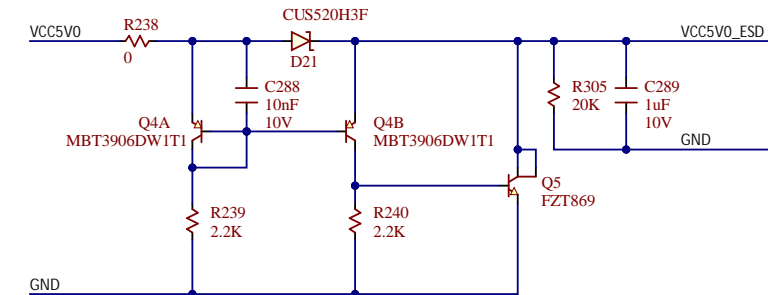
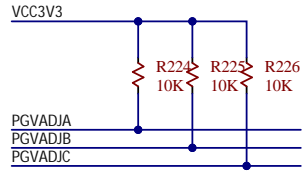
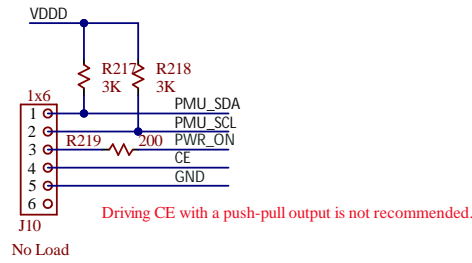
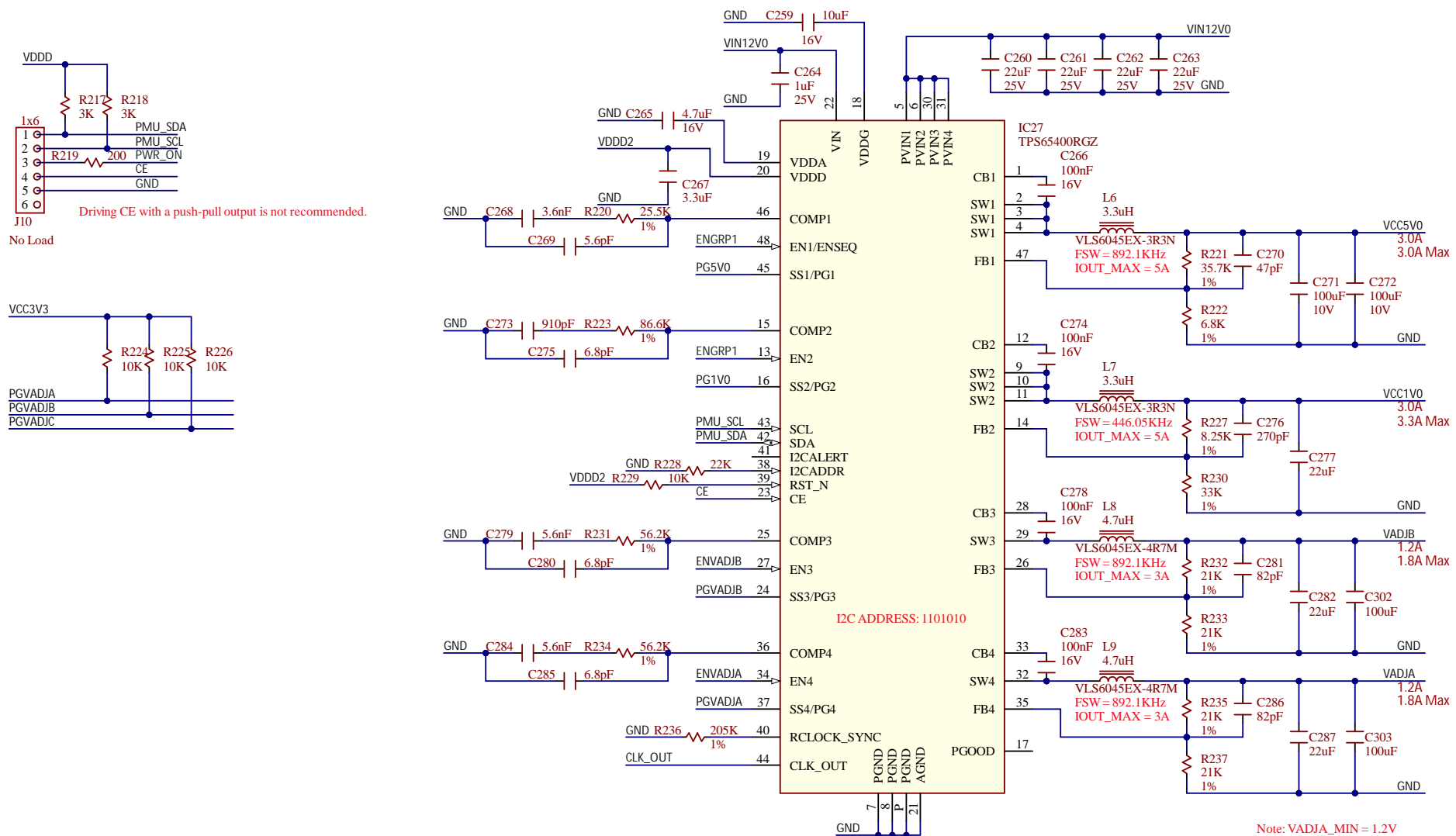
Note: VADJIC_MIN = 1.875V
 Note: VADJIC_DEFAULT = 2.5V
 Note: VADJIC_MAX = 5.84V

Note: our desired switching frequency is 892.1KHz, which would typically require a 205K resistor connected to RCLOCK_SYNC. However, because we want to synchronize to an external 892.1KHz clock we must use a resistor that sets the switching frequency approximately 30% lower than the external clock. Therefore we use a 300K resistor to set the internal switching frequency to 621.8KHz.

Title Eclypse Z7		Rev B.2
Circuit Power Regulation		
Doc#	500-393	
Engineer	MTA	
Author	GMA	
Date	10/28/2020	
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ISENSE_GAIN = 10A/V for all channels
 TON_RAMP_RATE = 0.25V/ms for all channels

Note: VADJA_MIN = 1.2V
 Note: VADJA_DEFAULT = 1.6V
 Note: VADJA_MAX = 3.74V

Note: VADJB_MIN = 1.2V
 Note: VADJB_DEFAULT = 1.6V
 Note: VADJB_MAX = 3.74V

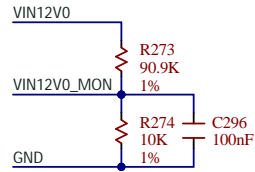
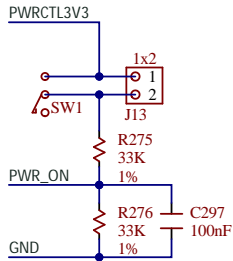
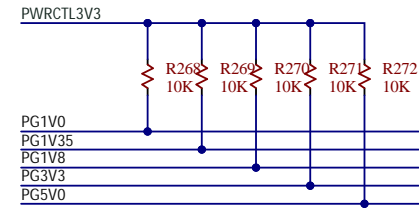
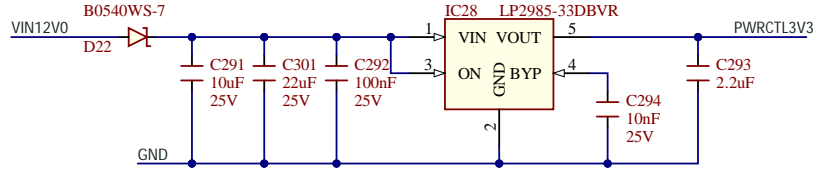
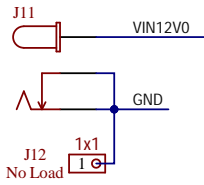
IC ADDRESS: 1101010

Title		Rev
Eclypse Z7		B.2
Circuit		
Power Regulation		
Doc#	500-393	
Engineer	MTA	
Author	GMA	
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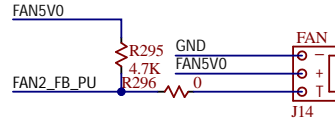
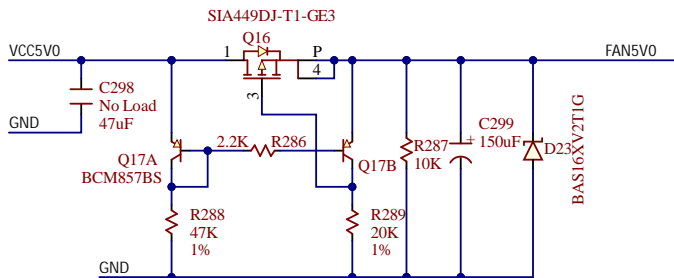
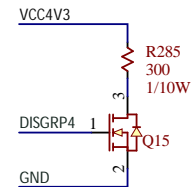
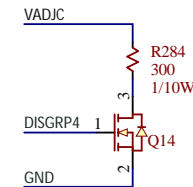
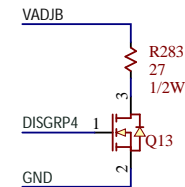
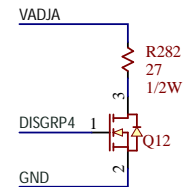
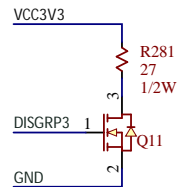
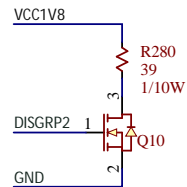
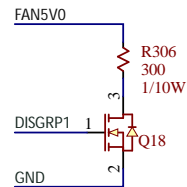
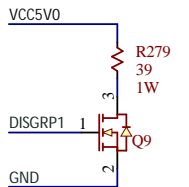
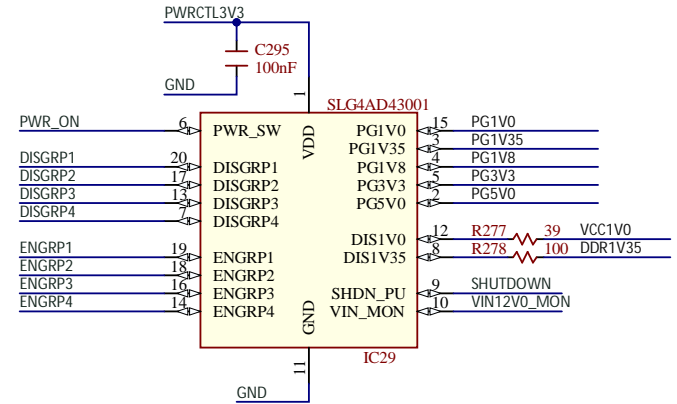
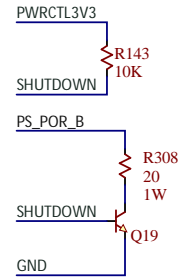


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Note: Input Voltage 12V only!



Input Voltage Enable Threshold			
	MIN	TYPICAL	MAX
TURN ON	10.038V	10.221V	10.407V
TURN OFF	9.791V	9.969V	10.150V



Title		Rev	
Eclypse Z7		B.2	
Circuit Regulation and Sequencer			
Doc#	500-393	Author	GMA
Engineer	MTA	Date	10/28/2020
Sheet#	15 out of 15	Copyright	2020