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B022412(022)

B. Tech. (Fourth Semester) Examination, April-May 2024

(New Scheme)

(Computer Science and Engineering Branch)

COMPUTER SYSTEM ARCHITECTURE

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Attempt all questions. Part(a) of each unit is compulsory. Attempt any two parts from (b), (c) and (d). Part(a)-4 marks, Part (b),(c), (d)-8 marks each.*

UNIT-I

1. (a) Define various general purpose and special purpose registers.

(b) Explain the different functional units of a computer

with the help of Block diagram?

(c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) index with R1 as the index register.

(d) Write the differences between hardwired and Micro programmed control unit.

UNIT-II

2. (a) Describe guard bits.

(b) Explain the design of fast adder for addition and subtraction by 2's complement.

(c) Explain Booth's Algorithm for multiplication of signed 2's complement numbers.

(d) Explain how various floating point arithmetic operations are performed in CPU.

UNIT-III

3. (a) Define multi-module memory.

(b) Draw and explain memory hierarchy. Explain different types of memory with neat diagram.

(c) Explain the working of associative memory with block diagram.

(d) What are the different types of mapping used in cache organization? Explain set associative mapping with example.

UNIT-IV

4. (a) Explain synchronous and asynchronous data transfer.

(b) Write the differences between IO mapped IO and Memory Mapped IO.

(c) Explain different types of interrupts and interrupt handling mechanism in detail.

(d) Explain the working of DMA with advantages and disadvantages.

UNIT-V

5. (a) Describe array processors.

(b) What do you understand by parallel processing.

Describe Flynn's classification of parallel processing.

(c) Specify a pipeline configuration to carry out arithmetic operation (Ai + Bi)(Ci + Di)

(d) Consider the execution of the program 15000 instructions a linear pipeline with a clock rate of 25 MHz. Assume that the instruction pipeline has 5 stages and that one instruction is issued per clock cycle. Calculate :

(i) Speed up factor (ii) Efficiency (iii) Throughput