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B022314(022)

B. Tech. (Third Semester) Examination, April-May 2023

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Part (a) is compulsory from each unit and carry equal 4 marks. attempt any* ***two*** *parts from (b), (c) and (d) from each question and carry equal 8 marks.*

Unit-I

1. (a) Convert the Boolean Expression $\overline{((A+B)C)}\,D$ using NAND gates only.

(b) Reduce the following function using Karnaugh map and implement using basic gates

$$f(A, B, C, D) = \overline{A}\overline{B}D + AB\overline{C}\overline{D} + \overline{A}BD + ABC\overline{D}$$

(c) Reduce the following equation using Quine Meclusky method of minimisation

$$F(A, B, C, D) = \sum m(0, 1, 3, 4, 5, 7, 10, 13, 14, 15)$$

(d) Do as directed :

(i) Convert $(2AC5{\cdot}D)_H$ to decimal, octal and binary

(ii) Solve $(DDCC)_{16} + (BBAA)_{16} = (\cdots\cdots)_{16}$.

Unit-II

2. (a) Define the following parameter.

(i) Noise margin

(ii) Power dissipation

(iii) Propogation delay

(iv) Fan out

(b) Draw the circuit diagram and explain the operation of 2-input TTL NAND gate with open collector output.

(c) Explain with neat diagram interfacing of a TTL gate driving CMOS gate and Vice versa

(d) Write short note on :

(i) PLA 4

(ii) PAL and FPGA 4

Unit-III

3. (a) Explain design procedure for combinational circuit.

(b) Draw and explain the block diagram of n-bit parallel adder circuit.

(c) Design 32 to 1 multiplexer using two 74LS150 ICs.

(d) Draw and explain circuit for 3 to 8 decoder.

Unit-IV

4. (a) What is race around condition? How it is avoided.

(b) Explain the working of 4 bit asynchronous counter.

(c) What are registers. Differentiate between Buffer Register & shift register.

(d) Design the counter that goes through state 1, 2, 4, 5, 7, 10, 11, 1 ..... using J-K flip flops.

Unit-V

5. (a) Define finite state machine.

(b) Differentiate between Mealy machine and Moore machine.

(c) What is VHDL. Give data flow and algorithmic and structural description.

(d) Write VHDL code to design 4 to 1 MUX.