MODBUS TABLE ORGANIZATION

Starting Address of the Group Registers (Dec)	Starting Address of the Group Registers (Hex)	System Version (Release)	System Version (Build)	Group Name (Text)	Group Code (Hex)	Group Complexity (Hex)	Group Version (Hex)	Object Code
4352	1100	01	16	Generic Output	11 00	10	01 00	
4352	1100	01	16	Generic Output Configuration	11 00	10	01 00	
16896	4200	01	16	Button State	53 01	10	01 00	

MODBUS PROTOCOL DETAILS

Function Code (Dec)	Exception Codes (Dec)	Data Encoding
2 (Read Discrete Inputs)	1, 2, 3	"Big Endian" (most significant byte first)
1 (Read Coils)	1, 2, 3	"Big Endian" (most significant byte first)
5/15 (Write Single/Multiple Coils)	1, 2, 3	"Big Endian" (most significant byte first)
4 (Read Input Registers)	1, 2, 3	"Big Endian" (most significant byte first)
3 (Read Holding register)	1, 2, 3	"Big Endian" (most significant byte first)
6/16 (Write Single/Multiple Holding register)	1, 2, 3	"Big Endian" (most significant byte first)

MODBUS OVER SERIAL DETAILS

Physical Layer	Trasmission Modes	Device Addressing	Baud Rates (bit/s)	Data Bits	Data bits trasmission sequence	Parity	Stop Bits
standard EIA/TIA 485 (RS-485) two-wire configuration	RTU	1÷247	programmable (1200, 2400, 4800, 9600, 19200, 38400)	8	Least significant bit first	NONE	1

MASTER/SLAVE COMMUNICATION TIMING

Timer Description	Timer Value (msec)
Inter-character time-out	< 1,5 character times
Response delay (from master request)	-
Delay Time (between two master trasmissions)	-

REFER ALSO TO: www.modbus.org
- MODBUS over serial line specification and implementation guide V1.02
- MODBUS APPLICATION PROTOCOL SPECIFICATION V1.1b

NOTE: File and printed copies of this document are not subject to document change control.

Register Number	Register Address (Dec)	Register Address (Hex)	Dimension [bit]	Description	Note	Read Function Codes (Dec)	Data Storing
16897	**16896**	**4200**	**2**	**Button State**			
16897	16896	4200	1	State of Button 1	*See Note 1*	2	
16898	16897	4201	1	State of Button 2	*See Note 1*	2	

Note 1
The information reported here "self-resets" when the condition that generated it ends.

Register Number	Register Address (Dec)	Register Address (Hex)	Dimension [bit]	Description	Note	Read Function Codes (Dec)	Write Function Codes (Dec)	Data Storing
4353	**4352**	**1100**	**2**	**Generic Output**				
4353	4352	1100	1	Activate Output 1		1	5,15	
4354	4353	1101	1	Activate Output 2		1	5,15	

Register Number	Register Address (Dec)	Register Address (Hex)	Dimension [word]	Bit Position	Description	Type	Scale	Unit	Range	Note	Read Function Code (Dec)	Data Storing
(no INPUT REGISTERS availables)												

Register Number	Register Address (Dec)	Register Address (Hex)	Dimension [word]	Bit Position	Description	Type	Scale	Unit	Range	Note	Read Function Codes (Dec)	Write Function Codes (Dec)	Data Storing
4353	**4352**	**1100**	**10**		**Generic Output Configuration**								
4353	4352	1100	1		Map Position of Output 1		-	-			3	6,16	
4354	4353	1101	1		Command Output 1 configuration		-	-		*See Note 3*	3	6,16	
4355	4354	1102	1		Activation Time of Command Output 1		0,1	sec			3	6,16	
4356	4355	1103	1		Delay activation Time of Command Output 1		0,1	sec			3	6,16	
4357	4356	1104	1		Interlock Output 1/Output x	register	-	-		*See Note 4*	3	6,16	
4358	4357	1105	1		Map Position of Output 2		-	-			3	6,16	
4359	4358	1106	1		Command Output 2 configuration		-	-		*See Note 3*	3	6,16	
4360	4359	1107	1		Activation Time of Command Output 2		0,1	sec			3	6,16	
4361	4360	1108	1		Delay activation Time of Command Output 2		0,1	sec			3	6,16	
4362	4361	1109	1		Interlock Output 2/Output x	register	-	-		*See Note 4*	3	6,16	

Note 3

bit0:
"0": Normally Open (NO)
"1": Normally Close (NC)

bit1|2:
"00": Implusive command
"01": toggle command
"10": maniteined command

bit3:
"0": Indipendent outputs
"1": Interlocked outputs

bit4÷15: not used

Note 4

"x" is the ID of the output interlocked (default 8000, the value of the register should be the address of the Coils of the output associated)